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REPORT NO. 3699
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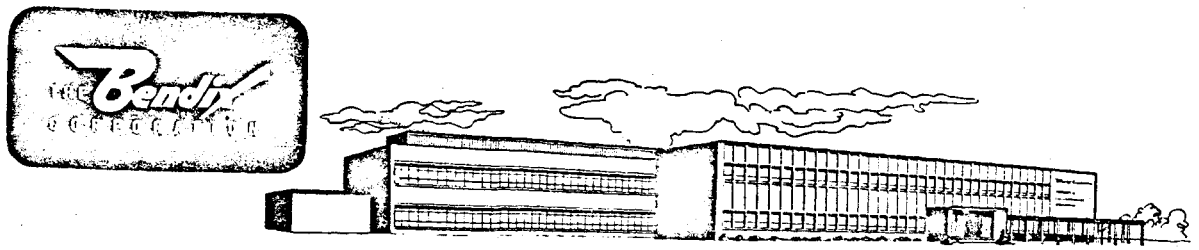
STUDY TO INVESTIGATE THE EFFECTS OF IONIZING RADIATION ON TRANSISTOR SURFACES

D. L. Nelson, R. J. Sweet, and D. J. Niehaus

FINAL REPORT

Contract NAS 8–20135
NASA/ George C. Marshall Space Flight Center



RESEARCH LABORATORIES DIVISION
SOUTHFIELD, MICHIGAN

K-1-46795

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January 1967

Submitted to

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama, PR-EC

Contract NAS 8-20135

The Bendix Corporation
Research Laboratories Division
Southfield, Michigan 48075

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ABSTRACT

Ionizing radiation effects, primarily in SiO_2 passivated bipolar transistors, were investigated. Changes in the electrical parameters of irradiated transistors, particularly h_{FE} and I_{CBO}, were studied first in order to determine the physical mechanisms in the surface that produce them. Then various types of devices were studied to determine the characteristics that produced their various degrees of radiation tolerance. The types of devices studied were: n-p-n and p-n-p bipolar transistors, transistors with commercial and experimental passivation processes, a p-channel MOSFET, and a p-channel junction FET. A nondamaging screening cycle was developed, which permits transistors to be exposed to ionizing radiation for evaluation of their radiation tolerance and then returned to their preirradiation conditions.

h_{FE} and I_{CBO} degradations in SiO_2 passivated transistors were demonstrated to be sensitive to bias and to the presence of an ambient gas during irradiation. Two mechanisms of surface degradation are prominent at low injection levels, and a third mechanism is effective at high injection. Buildup of h_{FE} degradation differs in n-p-n and p-n-p SiO_2 passivated planar transistors, with the n-p-n devices generally more radiation-tolerant. None of the three commercial passivation processes investigated--Fairchild's Planar II, Motorola's Band Guard, and Texas Instruments' Tri Rel--inhibited deleterious effects on h_{FE} and I_{CBO} due to ionizing radiation. A significant discovery was that experimental passivation, in which metallization was laid over the emitter-base junction, significantly reduced h_{FE} degradation and eliminated one of the low level damage mechanisms.

SECTION 1

INTRODUCTION AND SUMMARY

1.1 BACKGROUND

The degradation of desirable electrical properties of silicon transistors subjected to steady state radiation environments results from physical changes of the semiconductor material either in the bulk or at the surface of the semiconductor (between the semiconductor and the passivation layer or in the passivation layer of planar devices) or in both the bulk and at the surface. This report presents the results of an investigation of the radiation-induced surface effects in semiconductors.

There are two obvious reasons for studying ionizing radiation effects on transistor surfaces. The first is to identify the mechanisms producing the effects and to understand their dependence on materials, geometry, processes, and electrical operating conditions, so that techniques can be developed to reduce or eliminate the deleterious effects. The second is to identify and separate the transistor degradation that is dependent on surface properties from that which is dependent on bulk displacement phenomena. Bulk displacement effects in transistors are well understood and can be accurately described analytically.[1.1] Surface effects due to ionizing radiation are not well understood, and useful analytical relationships have not been developed. In addition, transistor degradation due to radiation-induced surface effects often predominates over bulk displacement effects for such environments as Van Allen belts in space and radiation from nuclear reactors, nuclear propelled vehicles, and nuclear space power systems.

1.2 OBJECTIVES

This program had three major objectives. The first was to study ionizing radiation effects in silicon, planar, SiO_2 passivated, bipolar transistors to achieve an understanding of the natural, physical processes (mechanisms) that occur near the surface. This study was to be accomplished by attempting to isolate the dominant degradation mechanisms and to determine the effects of electrical bias, temperature, and ambient media on them.

The second objective was to evaluate various transistor types and manufacturing processes to assess the relative merits of each with respect to its tolerance to ionizing radiation.

In the event that achievement of the first two objectives did not result in satisfactory solutions to surface degradation, the third objective was to develop a nondamaging screening test to permit determination of the relative ionizing radiation tolerance of transistors.

1.3 APPROACH

The program established to accomplish the desired objectives was basically experimental, and was divided into two separate phases. Phase I was devoted to the study of the effects of ionizing radiation in a single transistor type (the Fairchild 2N1613), which eliminated variables that would be introduced by different manufacturing processes. After the damage mechanisms of this device were understood, the investigation was extended to other device types and other manufacturers.

The source of radiation used throughout the program to simulate all types of steady state ionizing radiation was a 150 keV constant potential X-ray generator. This radiation source produces only ionizing effects since its maximum energy level is low enough that it cannot cause significant bulk displacement damage. As a result, all radiation damage observed is attributable to surface degradation.

The two transistor parameters affected by radiation-induced surface effects that are of most concern to the circuit designer are common emitter current gain h_{FE} and collector-base leakage current I_{CBO}. In this program, primary emphasis was devoted to changes in these two parameters due to the accumulated ionizing radiation exposure in units of roentgens (R). Dose rate (R/s) effects to these parameters were eliminated by removing the devices from the radiation field during measurments. Devices were usually irradiated for a period of time, removed from the radiation source for several minutes to make measurements, then returned for additional radiation. Such radiation-measurement cycles continued until the device received the total desired accumulated dose. The number of cycles depended on the number of data points desired. Usually several points were taken at both low and high accumulated doses. Data were usually plotted to show damage as a function of total radiation exposure dose.

In Phase I, 2N1613 transistors were subjected to ionizing radiation with various electrical biases. The effects of these electrical and radiation stresses on h_{FE} and I_{CBO} were determined for various values of collector current during measurement. Similar experiments were performed with 2N1613s subjected to stresses of temperature and radiation, temperature alone, and radiation and various ambient media surrounding the transistor surface, i.e., air, vacuum, and dry nitrogen. These experiments were designed to provide data for identifying the surface damage mechanisms and for developing a theoretical model to describe radiation-induced surface effects. The experiments with temperature, radiation, and electrical bias were performed to evaluate various techniques for screening transistors for their tolerance to ionizing radiation, i.e., separating, by nondestructive methods, devices with good surface stability in radiation from those with poor surface stability.

Phase II was essentially a device evaluation phase intended to verify the theories and the screening techniques developed in Phase I and to determine the influence of fabrication and surface passivation processes on

radiation induced surface effects. The processes evaluated for bipolar transistors included planar SiO_2 passivated, epitaxial-mesa, mesa, alloy junction, Fairchild's Planar II, Texas Instruments' Field Plate, Motorola's annular (band-guard process), and two experimental processes wherein metallization was placed over the emitter-base junction. Both n-p-n and p-n-p transistors were evaluated as well as junction and metal-oxide-semiconductor field effect transistors.

Experiments performed on the device types enumerated above not only provided a comparative evaluation of their ionizing radiation tolerance but also provided an evaluation of the screening technique and the damage model for a wide variety of devices.

1.4 SUMMARY OF RESULTS

The two major achievements of the program were: (1) the determination of the damage mechanisms involved in transistor surface radiation effects and the dependence of these mechanisms on certain electrical conditions, temperatures, ambient media, device construction, and surface treatments; and (2) the development of an effective nondestructive screening technique for separating transistors with good surface stability in ionizing radiation from those with poor surface stability.

The surface properties of SiO_2 passivated silicon devices exposed to ionizing radiation change due to a net accumulation of positive charge over the SiO_2-Si interface. The charge accumulation or redistribution in the SiO_2 layer results from migration of ionized charge carriers under the influence of electric fields in the SiO_2. For MOSFET devices, these fields result from an applied gate potential, and, for junction devices, from junction fringing fields and ionized gas charge collection on the SiO_2-ambient surface. The charge accumulation over the SiO_2-Si interface changes the semiconductor surface potential, surface recombination velocity, and surface carrier concentration, and these changes in turn produce changes in h_{FE} and I_{CBO}. The amount of degradation is dependent upon the electrical bias conditions during irradiation, since these conditions influence the magnitude of the electric fields in the SiO_2 layer.

A reverse biased collector-base junction during irradiation can cause ionized gas charge to collect on the SiO_2-ambient surface, which results in inversion of the p-material and lateral extension of the base-emitter and collector-base junctions beneath the SiO_2-Si interface. The effect of this channel on h_{FE} and I_{CBO} varies widely depending on the quality of the silicon directly beneath the SiO_2-Si interface. A channel which extends to a gross defect or "generation site" at the interface, can result in a catastrophically large current, while a relatively clean interface produces only minor changes in I_{CBO} and h_{FE}. Another cause of degradation is surface space charge region recombination-generation current which is produced by a decrease in the surface potential. The lower silicon surface potential enlarges the area of the space charge region-SiO_2 interface and increases surface recombination velocity which

results in a higher probability of recombination-generation in the space charge region. The effect of channel current and surface recombination-generation current is very pronounced at low measurement or operating currents where the surface contribution to the base current is relatively large. Large changes in h_{FE} and I_{CBO} occur at low operating currents for doses as small as 10^4R. The damage effects tend to saturate or even recede at high doses due to channel recession. Damage saturation generally occurs between 10^5 and 10^6R.

Transistors irradiated without bias applied to either junction have a lower rate of damage buildup and a lower magnitude of damage with radiation dose than reverse-biased transistors. Magnitudes and rates of damage are also smaller at higher measurement currents. The same is true for transistors with forward-biased junctions where the magnitudes and rates are lower than the zero bias case.

In summary, both the magnitude of damage and rate of damage buildup with dose are greatest for the case of reverse bias during irradiation. They are smaller when irradiation takes place without bias and are smallest when transistors are forward biased during irradiation. For any bias condition, damage and damage rate become smaller as the measurement or operating currents become larger. Damage buildup can be appreciable at 10^4R and generally reaches a saturation level by 10^6R.

The major difference between p-n-p and n-p-n transistors is in the formation and recession of the channel. n-p-n transistors experience channeling and rather rapid buildup of damage at relatively low doses, but at high doses the channel recedes and damage saturates or in some cases recedes to lower levels. For p-n-p transistors, the damage builds up more slowly at low doses but continues to increase with dose rather than receding as in the case of n-p-n transistors.

The ambient medium (gas or vacuum) surrounding the transistor influences radiation surface damage. No large differences in damage occur between the normal nitrogen ambient and a vacuum for devices with passive or forward biases during irradiation. However, for reverse bias conditions, damage buildup with dose is considerably less at low doses for evacuated devices than for those with nitrogen ambient. At high doses ~ 10^7R, differences in magnitude of damage between vacuum and nitrogen ambient are small. Evacuation is therefore an effective means of reducing damage to reverse-biased transistors at low doses, 10^5 to 10^6R, because it reduces the effect of channeling. It is not a remedy for all surface damage since other damage mechanisms are present which are not affected by the ambient.

High temperatures can be used very effectively to remove surface damage induced by radiation. Experiments showed that radiation-induced surface damage in SiO_2 passivated transistors can be removed by baking the transistors at about 300°C for a period of five hours. The ability to recover transistors to their initial conditions enables screening of

device types and selection of individual transistors which are least susceptible to damage by ionizing radiation. Transistors are first irradiated with X-rays to establish their behavior in ionizing radiation so that the least susceptible devices can be screened from the more susceptible ones. The selected devices can be restored to their preirradiation values by the 300°C baking period.

The temperature recovery technique also permitted the use of series-testing in the investigative experiments of Phase I. Single devices were irradiated under a variety of conditions with the damage removed by annealing after each test condition. Series-testing prevents variations among devices from influencing the results of the comparison.

The device evaluation experiments indicate that there are no significant advantages of p-n-p over n-p-n transistors subjected to ionizing radiation environments. Even though the magnitude of the channel damage component was higher in some n-p-n's than in p-n-p's at doses on the order of 10^5R, there is no conclusive evidence that the h_{FE} degradation rate in general is significantly less in the p-n-p transistor. Various techniques for eliminating increases of p-n-p I_{CBO}, such as a p^+ annular ring (Motorola's annular process) or a metallization over the collector base junction (Texas Instruments' field plate) do not produce transistors that are immune to ionizing radiation. The TriRel process (Texas Instruments), which includes a field plate, a p^+ doped guard ring, and a P_2O_5 getter for sodium and potassium ions, also failed to produce a transistor that is immune to ionizing radiation. The Fairchild Planar II process provides transistors with excellent initial surface interface characteristics; nevertheless it was unable to inhibit surface damage.

Other results show that attempts by two manufacturers to inhibit h_{FE} degradation by placing metallization over the emitter-base junction proved effective in eliminating the dominant channel current mechanism of h_{FE} degradation at low doses. (No bias was required on the metallization; various biases proved to be ineffective.) Although this technique eliminated the channel mechanism, h_{FE} degradation did not completely disappear because other damage mechanisms were still prevalent. However, h_{FE} spreads and total incurred damage were smaller in the metallized transistors than in the same devices without metallization. This method of reducing damage buildup differs from screening in that it completely avoids the channel mechanism. Moreover, the tight grouping of h_{FE} spreads it produces implies that metallization and careful process control will ultimately preclude requirements to screen.

Additional experimentation and evaluation of both radiation-temperature screening and emitter base metallization techniques are required to achieve transistors with minimum susceptibility to ionizing radiation.

The final experiments on field effect transistors revealed that MOSFETs are extremely vulnerable to ionizing radiation. Drain-source leakage current increased five decades, from 100pA to 10μA, for a dose of 2.5×10^4R when the p-channel MOSFET was biased ON during irradiation. The magnitude of the required negative gate voltage to turn on the MOSFET increases with dose because of the positive charge buildup in the oxide.

For MOSFETs biased OFF during irradiation, the drain-source leakage current is a function of the applied gate voltage; however, most MOSFETs could not be turned on with the maximum allowable gate voltage after only 2.5×10^4R. After an accumulated exposure to about 10^6 to 10^7R, MOSFETs recover somewhat although electrical parameters are much different from their preirradiation values.

Experiments with p-channel junction FETs indicated that these devices have good tolerance to ionizing radiation. The transconductance of these devices was unaffected by radiation. Drain-source leakage current increased about a decade from 1 to 10nA after 1.5×10^6R, but the pinchoff voltage was unaffected by the radiation. Leakage current decreased slightly after 10^7R.

SECTION 2

EXPERIMENTAL PROGRAM

2.1 PHASE I

2.1.1 Causes of Degraded Gain and Increased Leakage Current

Ionizing radiation induces changes in the surfaces of SiO_2 passivated transistors that result in degraded h_{FE} and increased I_{CBO}. Phase I of the program was designed to provide an understanding of the mechanisms that produce these degradations and to develop techniques to be used in Phase II for nondestructively screening devices to identify those that are least susceptible to degradation by ionizing radiation. The experimental portion of this phase of the program was designed to provide the data necessary to determine the relationships between the induced degradation and various electrical and environmental stresses on transistors. Each Phase I test was planned largely from the results of previous tests, in line with the experimental nature of the program. Phase I was an investigative phase during which many different stresses were applied to a single device type to identify and determine the effects of various conditions on damage mechanisms. The mechanisms are discussed in Section 3.

In the initial stages of the program, attempts were made to eliminate as many variables as possible that would not aid in understanding the damage mechanisms. For this reason, Phase I of the program was restricted to the study of a single, planar SiO_2 passivated device type, the Fairchild 2N1613, which was arbitrarily selected. The effects of ionizing radiation were investigated for various conditions of electrical bias during radiation and during measurement, and various temperature, dose rates and ambient media. Changes in h_{FE} and I_{CBO} were observed as a function of radiation dose. The effects evaluated are summarized below.

2.1.1.1 Electrical Bias Effects During Irradiation

Biases applied to transistors during irradiation were: passive (no bias); collector-base junction reverse biases of 6V, 12V, and 50V; emitter-base reverse bias of 3V; and an active bias of 6V collector-base voltage and 10mA collector current (normal amplifier operating mode).

2.1.1.2 Electrical Bias Effects During Measurement

The effects of various measurement currents on damage were investigated by measuring h_{FE} over seven decades of collector current from 100nA to 300mA.

2.1.1.3 Temperature Effects

During data measurement, temperature normally was controlled at 35°C to avoid variations in damage response due to temperature differences. Temperature coefficient of damage was studied by making measurements at two controlled temperatures, 0° and 35°C.

Additional experiments were performed to determine the correlation, if any, between temperature and radiation induced h_{FE} degradation. Various reverse biases were applied to both the emitter-base and the collector-base junctions of test transistors, which were then subjected to temperatures as high as 300°C for as long as one hour. Some transistor manufacturers employ similar high temperature stress periods, referred to as "burn in," during which they monitor for instabilities in surface properties. Highly reliable transistors that do not use a gold-aluminum metal system generally are unaffected by temperature excursions to 300°C. (Gold-aluminum bonds subjected to long periods of high temperature stress can incur permanent chemical damage known as "purple plague.")

2.1.1.4 Rate Effects

The ionizing radiation dose rate generally used throughout the experiments was $\phi = 5 \times 10^5$ R/hr. Rate effects were investigated by means of rates of one-tenth and one-one hundredth of the normal dose rate.

2.1.1.5 Ambient Media Effects

Transistors are normally packaged in cans with a gas such as nitrogen or dry air as the ambient medium. The experiments discussed above were performed with transistors in their normal medium. Additional investigations were made of the effects of radiation stresses on transistors in vacuum and in room air.

2.1.2 Damage Removal Techniques

An additional goal of Phase I was to study various methods of damage removal and to develop a recovery technique whereby transistors that incur surface degradation can be returned to their preirradiation conditions. Such a technique is essential to the concept of screening devices for their tolerance to ionizing radiation and is, in addition, a valuable aid in the identification of damage mechanisms because it permits the same device to be tested in series under different conditions.

Series tests are important for eliminating the sensitivities of individual devices from the damage induced by a particular stress. Most of the initial experiments were performed on a parallel basis; i.e., 2N1613 transistors were divided into groups which were subjected to different stress conditions simultaneously. The qualitative results obtained from these experiments allowed identification of several damage mechanisms

and indicated the dominent damage mechanisms as functions of bias and dose. However, the relative magnitudes of damage induced as a function of stress during radiation could not be determined accurately from the parallel tests because each transistor has a slightly different sensitivity to each particular bias-radiation stress. Such comparisons could be made by means of series tests in which only a few transistors are subjected to alternate periods of bias-radiation stresses if a technique were available for removing the damage after each test. To develop such a technique, transistors were tested under experimental conditions of radiation, bias-radiation, bias-radiation-temperature, and finally high temperature stresses only. The results of these experiments were used to determine which stress or combination of stresses is most effective in removing ionizing radiation-induced damage and allowing the transistor to recover to its original condition.

2.2 PHASE II

The object of Phase II of the program was to extend the results of Phase I to transistor types other than the Phase I test device. The knowledge obtained in Phase I aided in developing procedures employed in Phase II to investigate the damage mechanisms of several n-p-n and p-n-p bipolar and two unipolar transistors. For the most part, a single bias-radiation stress was used on all device types investigated. Attempts were made to show that the damage mechanisms detected in Phase I were present in all the other devices also by using the bias that was most effective in developing damage in the 2N1613 devices of Phase I. The reverse-biased collector-base junction was effective in eliciting both the low-level damage mechanisms that are introduced in Section 3. The tests of Phase II, unlike those of Phase I, used fixed radiation and measurement procedures, fixed data measurement points, and fixed sample sizes. Among the devices tested were several experimental types that had been fabricated by techniques that were expected to reduce or eliminate device sensitivity to surface damage. To evaluate the screening technique developed in Phase I, each of the Phase II tests consisted of two cycles so that damage buildup in both cycles could be compared for repeatability.

2.3 GENERAL EXPERIMENTAL PROCEDURES

Experimental test procedures evolved from observations made during prior tests. To eliminate temperature effects while studying the effects of other stress parameters, temperatures were carefully controlled with an electronic temperature controller during data measuring cycles. In early tests it was discovered that the amount of h_{FE} degradation was less in a repeated measuring cycle than in the first measuring cycle, clearly indicating that damage was annealed by the measurement cycle. The amount of damage annealed appeared to be dependent upon the bias used during radiation. Damage was observed to anneal also as a function of shelf time (time during which devices remain in storage with no applied stresses other than ambient conditions). Consequently, the procedure for recording

data was modified to include a second reading of only the $1/h_{FE}$ datum at 10^{-7}A (the lowest measurement current available on the low level $1/h_{FE}$ tester) to be used to indicate the stability of induced degradation. All data point readings were recorded as soon as possible following removal of devices from the X-ray machine to avoid time annealing.

The general procedure developed for Phase I experiments was to record several closely spaced data points (a data point refers to all desired data subsequent to a specified amount of accumulated dose) at small doses and to record fewer data points as larger doses were accumulated; this was necessary due to the relatively large changes in transistor parameter degradation at early doses. Data recorded were generally $1/h_{FE}$ for $10^{-7} \leq I_C \leq 3 \times 10^{-1}$A and I_{CBO} at $V_{CB} = 5.3$V. Various other data were recorded in attempts to find changes in device parameters that would lead to identification of damage mechanisms. Junction capacitance data, which were recorded in some tests at each data point, were useful for indicating changes in junction geometry as a function of dose. Reverse-biased junction V-I characteristics were recorded in some instances, but were of no value for damage mechanism identification.

2.4 EXPERIMENTAL EQUIPMENT

2.4.1 Radiation Source

The ionizing radiation source employed in the program was a Siefert Isovolt 150kV constant potential X-ray generator. The maximum energy level developed is 150keV, with an average level of approximately 90keV. The advantage of using this source of ionizing radiation is that the X-ray energy is below the threshold for producing bulk displacement damage in transistors, but still sufficient to produce the desired level of ionizing radiation. An X-ray source has the added advantage of being a convenient, inexpensive laboratory facility for irradiating transistors. A photograph of this facility is presented in Figure 2-1. Another photograph in Figure 2-2 shows the test transistors mounted around the circumference of the X-ray tube inside the shielded enclosure.

The dose rate $\dot{\phi}$, as determined by thermoluminescent dosimeters from Controls for Radiation, Inc., was approximately 5×10^5R/hr for transistor dies enclosed in T05 and T018 cans. The dose rate delivered to power transistors was approximately 10^5R/hr because of their more massive package and because of their greater radial distance from the radiation source. Dosimetry measurements were taken by dosimeters enclosed in transistor cans placed at various distances, radial angles, and positions above and below the centerline of the beam of the X-ray source (Refer to Figure 2-3). Other dosimeters not enclosed in cans were placed within the radiation field so that the attenuation due to the cans could be determined.

The T05 and T018 cans attenuate the dose about 10 percent.

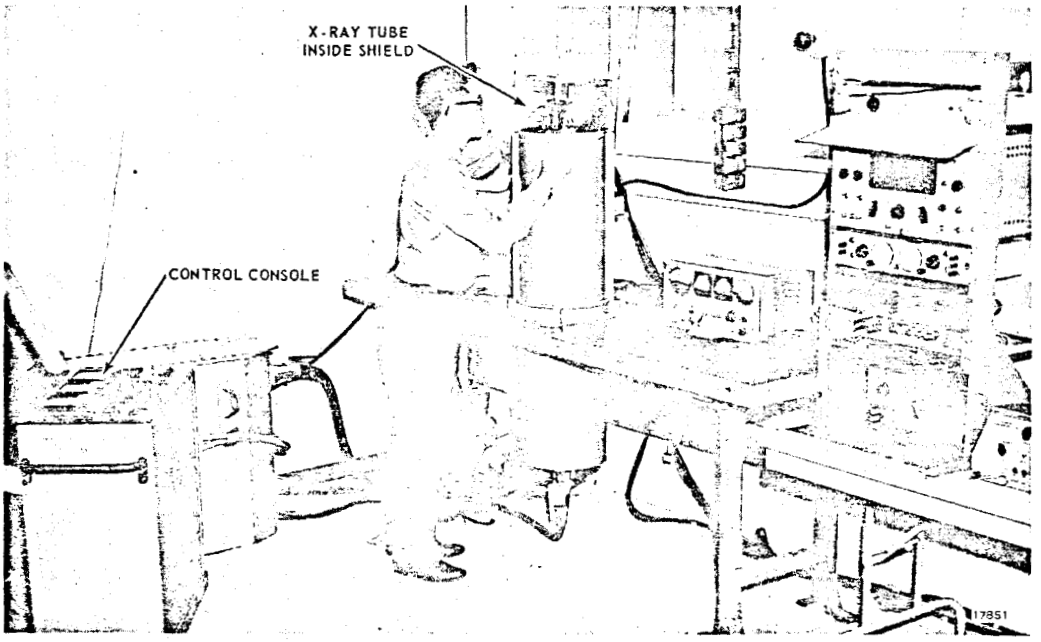


Figure 2-1 - X-ray facility

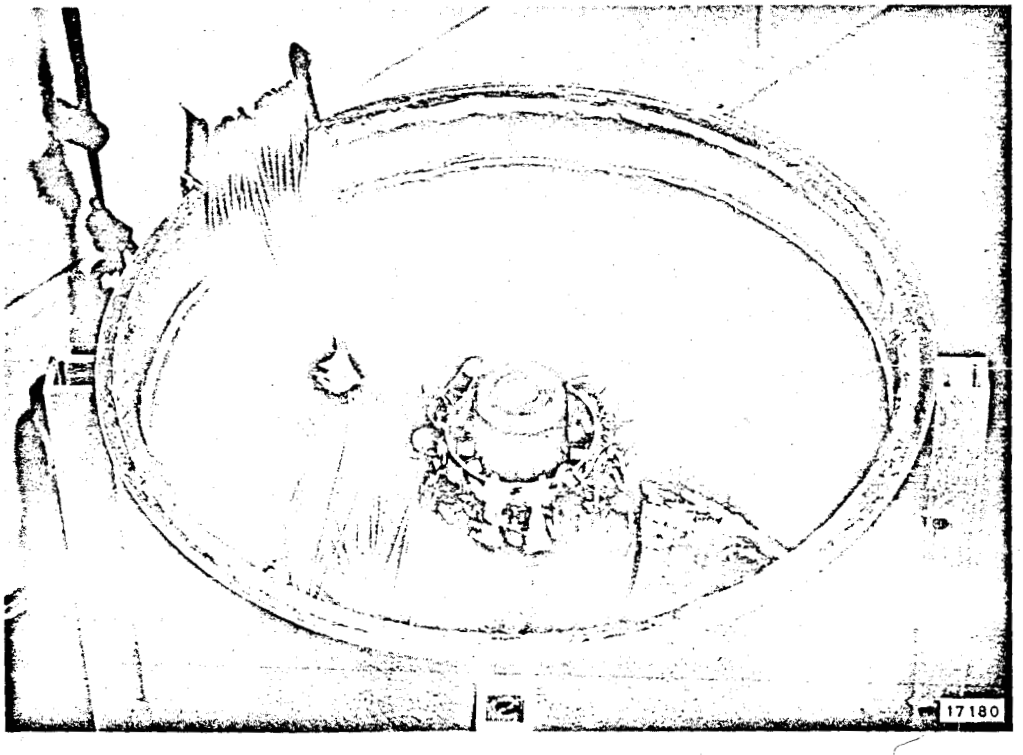


Figure 2-2 - X-ray tube mounted in its shield with transistors in place around the tube in preparation for irradiation

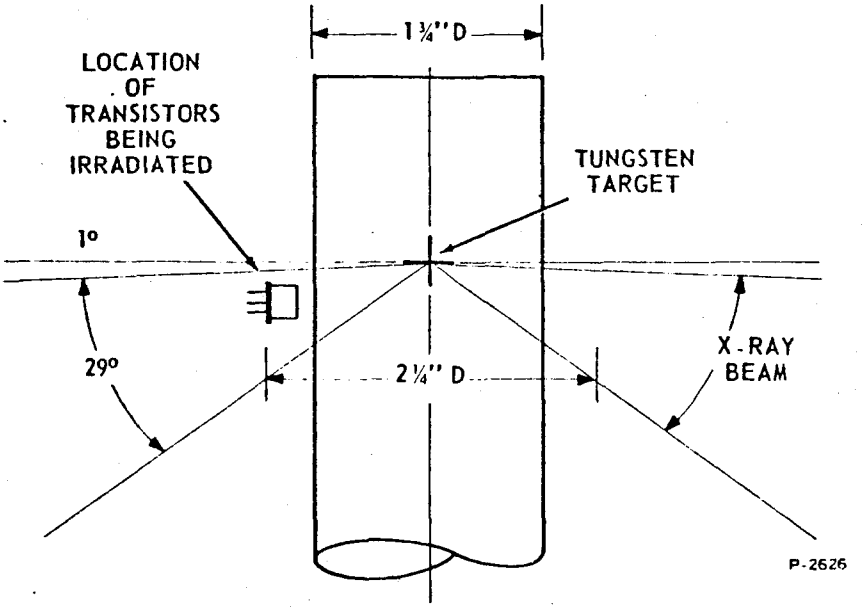


Figure 2-3 - X-ray beam geometry

2.4.2 Low Level $1/h_{FE}$ Tester

A special $1/h_{FE}$ tester was designed to measure gain degradation at low to medium collector currents (0.1μA to 100mA). This tester maintains I_C constant over the current range of interest, and a sensor measures the base current over the range of 50pA to 100mA. The accuracy of $1/h_{FE}$ readings varies from ± 5 percent at I_C = 0.1μA to < ± 0.2 percent at $I_C \geq$ 10μA. V_{CB} variations during measurements are too small to affect h_{FE}.

Large values of collector leakage current I_{CBO} can seriously distort the $1/h_{FE}$ versus I_C relation at low measurements because the actual measured base lead current includes I_{CBO}. The effect of I_{CBO} is partially compensated for in this system by inducing a current equal and opposite to I_{CBO} into the base lead. An equal compensating current is also fed into the collector side of the collector-base junction to compensate for the effect of I_{CBO} on collector current and allow the collector current control loop to maintain constant collector diffusion current.

An important feature of this tester is its capability of taking measurements using a single 75 $\pm$ 25ms measurement pulse which reduces electrical annealing of surface damage while data are being obtained from the test transistors.

2.4.3 High Level h_{FE} Tester

At collector currents from 1mA to 30A, a high current pulsed gain tester (Birtcher No. 70) was used. This tester utilizes a pulse train with a 2 percent duty cycle and a pulse width of 200μs. The accuracy of the tester is 2 percent of full scale h_{FE} readings, where full scale is either 100 or 1000.

2.4.4 Temperature Controller

During data measurements, temperature was controlled with a Peltier junction temperature controller capable of controlling junction temperatures within less than 1°C, thereby producing repeatable test conditions. The temperature coefficient of V_{BE} is approximately -2.7 mV/°C at I_C = 1μA and -2.1mV/°C at I_C = 1mA. Recorded data show that variations of V_{BE} were sometimes as much as 3mVbut were usually less than that.

2.4.5 Junction Capacitance Measurements

Junction capacitances were measured with a Wayne-Kerr Model B201 impedance bridge. The bridge has an accuracy of ±0.1 percent ± 1 minor division (fourth significant figure) and is capable of reading capacitance from 1pF to 0.01μF.

2.4.6 Reverse V-I Characteristics

Reverse junction V-I characteristics were plotted using a Hewlett-Packard analog plotter. Sweep and reverse bias voltage was supplied from the sawtooth generator of a Tektronix oscilloscope. The reverse current was measured with a Hewlett-Packard Model 425A dc Micro Volt- Ammeter and converted internally to a proportional voltage which was then fed into the vertical input of the plotter. The plotted curves have an accuracy of ±5 percent.

2.4.7 Logarithmic Amplifier

Special instrumentation was developed for FETs to allow measurement of drain current as a function of gate voltage from 10^{-10} to 5×10^{-3}A. This equipment utilizes a logarithmic amplifier with peak values of noise on the order of ±25pA. A system composed of this amplifier and an analog x-y recorder is capable of recording current-voltage characteristics with accuracies within ±5 percent over the entire operating range of the devices tested.

SECTION 3

DAMAGE MECHANISMS DETECTION AND IDENTIFICATION

3.1 INTRODUCTION TO SURFACE DAMAGE MECHANISMS

One source of surface instability normally associated with silicon dioxide passivated transistors is the physical dissimilarities between the oxide and silicon. The effects of SiO_2 passivation is a depletion of majority carriers in p-type material (or an enhancement of majority carriers in n-type material) beneath the oxide which can affect electrical performance. Likewise, ionization can affect electrical performance. X-ray irradiation causes ionization of the gas ambient surrounding the transistors or in the oxide itself, with a resulting charge buildup on and in the oxide similar to charge buildup observed in studies of high temperature effects.[3.1] These high temperature studies showed that the charge buildup results in apparent mobile charged species migration due to the electric fields that are set up and that eventually the charge buildup and migration change the character of the silicon dioxide and the silicon beneath the oxide and hence the electrical properties of the transistor. The charge buildup in the oxide is analogous to the applied gate potential of MOS structures; a positive potential on the gate causes an increase of electron density in the silicon beneath the oxide, while a negative potential causes an increase of hole density.

Charge buildup in or on the oxide of a passivated transistor causes the following changes in the silicon in the oxide-silicon interface region.

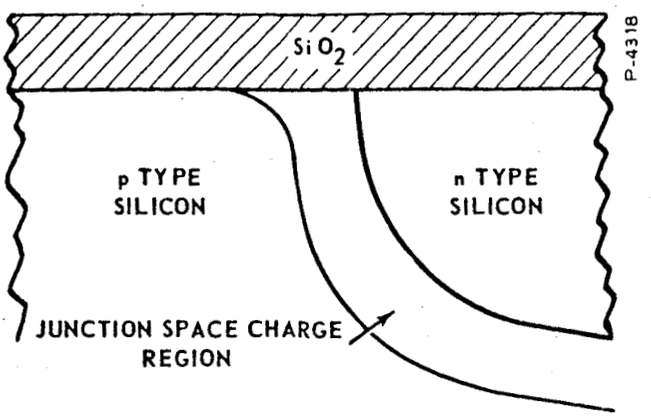
(1) Enhancement of the majority mobile charge carriers if the resulting potential of the surface oxide is of the opposite polarity to majority carriers.

(2) Depletion of the majority carriers if the resulting potential of the surface oxide is of the same polarity as the majority carriers.

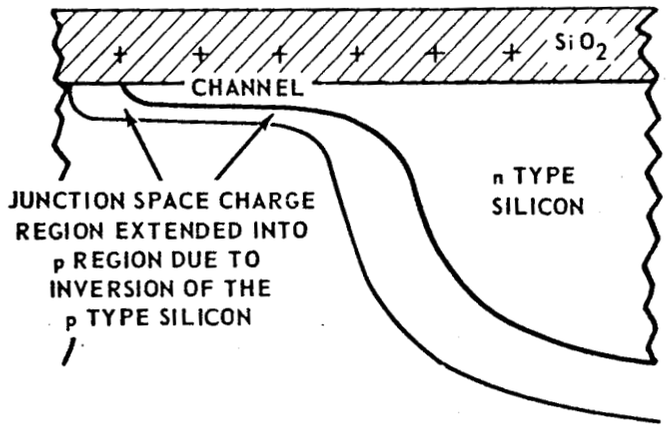
(3) Finally, if the oxide charge is strong enough to produce sufficient depletion to cause the minority carriers to dominate over the majority carriers in the surface region of the silicon, the silicon is said to be inverted.

When material is inverted in a junction region, the junction becomes extended, as shown in Figure 3-1, and a channel is formed. The term channel, as used in this report, refers to any extension of a junction without specifying a particular length or involvement of a junction contact.

Charge buildup in the oxide also affects the surface recombination velocity. The maximum recombination velocity occurs when electrons and holes recombine at the same rate. Silicon dioxide passivation enhances



(a) Normal p – n junction configuration



(b) Positive charge buildup in the SiO_2 layer causes inversion of p material beneath the layer and extends the junction

Figure 3-1 - p-n junction configuration for normal and channel conditions

n-type silicon and depletes p-type silicon. Positive charge building up in the surface oxide continues to enhance the n-regions and to deplete the p-regions so that the maximum recombination velocity is reached in the p-region as inversion is approached. The effects of increased recombination velocity are discussed in Sections 3.2 and 3.3.

The extended junction that occurs with inversion of the bulk material may be accompanied by increased junction capacitance. This increased capacitance results from the expanded junction surface area and the decreased junction width near the surface. The width of the junction decreases near the surface in diffused transistors because of the higher concentration of mobile charge carriers near the surface,

which is characteristic of the diffusion process. The space charge width has an inverse relation to the concentration of mobile charge carriers on both sides of the metallurgical junction.

3.2 INFLUENCE OF SURFACE CHANGES ON ELECTRICAL PARAMETERS

Two electrical parameters, h_{FE} and I_{CBO}, were selected for study in this program because of their sensitivity to surface changes. Junction capacitances were also monitored in most experiments because they can be good indicators of damage mechanisms. Changes in junction capacitance due to radiation-induced channels are discussed in Section 3.1.

Changes in the current gain of a transistor due to radiation can best be analyzed by examining the various current components that determine current gain. Consider first a transistor biased in the common emitter mode with forward-biased emitter-base and reverse-biased collector-base junctions. The basic current components are:

(1) I_D, the diffusion current component from the emitter into the base due to the heavily doped emitter region and the forward biased base-emitter junction.

(2) I_D', the reverse diffusion component from the base into the emitter (a much smaller component than I_D because the base is doped lower than the emitter).

(3) I_{RB}, the base bulk recombination current, made up of those minority carriers injected from the emitter that, in diffusing across the base, recombine and are lost before reaching the collector.

(4) I_{RG}, the recombination-generation component resulting from generation sites in the emitter-base space charge region.

(5) I_{SRG}, the surface recombination-generation component of injected carriers that results because the junctions extend to the Si-SiO_2 interface region where many generation sites exist.

(6) I_{CBO}, the collector-base leakage current composed principally of the recombination-generation current in the collector-base space charge region.

The gain h_{FE} is the ratio of the collector current (diffusion current I_D plus leakage current I_{CBO}) to the base current I_B. I_B is composed of I_D', I_{RB}, I_{RG}, I_{SRG}, and I_{CBO}. Irradiation causes additional base current components to appear and other components to increase in magnitude. Channel current I_{CH} occurs as a result of the inversion process discussed above. The magnitude of the I_{CH} component is a function of the number of generation sites in the channel region, which is a function of the quality of the SiO_2 and of the chemical structure of the interface. Also, the I_{SRG} component increases with the induced charge

buildup in the oxide because ionizing radiation increases the surface recombination velocity.

The two radiation-sensitive components, I_{CH} and I_{SRG}, dominate h_{FE} at low injection levels and can therefore produce large changes in gain at low currents. At high injection levels, the base current spreads away from the center to the periphery of the base due to the transverse voltage developed across the base spreading resistance and hence is affected more by conditions at the surface. I_{RB} increases because of the surface recombination-generation sites that increase the probability of recombinations in the base. As radiation-induced charge builds up in the oxide inducing a channel, the concentrations of majority carriers on both sides of the junction tend to approach the same magnitude, thereby increasing the surface recombination velocity. The reverse diffusion component I_D' becomes large and emitter efficiency drops off, thus reducing h_{FE}.

For convenience the effects of the various base current components of h_{FE} at both low and high injection levels are analyzed in the form of the reciprocal h_{FE} so that the base currents appear in the numerator. At low injection, reciprocal gain can be written:

$$\frac{1}{h_{FE}} = \frac{I_B}{I_C} = \frac{I_D' + I_{RB} + I_{RG} + I_{SRG} + I_{CH} - I_{CBO}}{I_C} \tag{3.1}$$

The influence of the radiation-induced I_{CH} and I_{SRG} components on gain was determined by subtracting the leakage current component I_{CBO} from the gain measurements and eliminating it from the gain expression, equation (3.1). Leakage current changes were studied separately by independent leakage current measurements. In this way the damage mechanisms affecting gain and leakage current were isolated and studied independently.

The radiation-affected components are separated from the nonaffected ones by

$$\frac{1}{h_{FE}} = \frac{I_{BO} + I_{SRG} + I_{CH}}{I_C} \tag{3.2}$$

where I_{BO} is the sum of base current components, excluding I_{CBO}, of equation (3.1) that are unaffected by changes in the surface properties.

At high injection, I_{CH} and I_{SRG} are small and can be ignored. $1/h_{FE}$ at high injection can therefore be written from equation (3.1) as follows:

$$\frac{1}{h_{FE}} = \frac{I_{BO} + I_{SD}' + I_{SRB}}{I_C} \tag{3.3}$$

where I_{BO} is as defined above and I'_{SD} and I_{SRB} are surface components of I'_D and I_{RB}, respectively, which are affected by ionizing radiation.

Increases in I_{CBO} are a result of channel currents and surface recombination-generation currents at the base-collector junction. The reverse-biased junction has a reduced carrier concentration because of the bias, and the p material is more easily inverted with positive charge buildup in the oxide. Channel formation by inversion occurs in the surface region where the number of generation sites is relatively large due to the imperfect chemical structure at the SiO_2-Si interface region. Thus the I_{CH} and I_{SRG} components are readily enhanced. Figure 4-6 shows a comparison of the I_{CBO} characteristics of two 2N1613 transistors as a function of radiation time. The relatively poor interface region with more generation sites in transistor 8 is evidenced by the fact that I_{CBO} is two decades larger in transistor 8 than in transistor 15 at an exposure of $\phi \doteq 6 \times 10^4$R.

3.3 IDENTIFICATION OF DAMAGE MECHANISMS

The excess current components that occur as a result of surface damage have characteristics that vary exponentially with forward emitter-base bias voltage V_{BE} as follows:

$$I \propto e^{\frac{q\,V_{BE}}{n\,kT}} \qquad (3.4)$$

The factor n is a slope constant which takes on different values depending upon which damage mechanism is dominant[3.2, 3.3]. The factor n is therefore a very useful detector of the dominant mechanism; however, since several damage mechanisms can affect transistor electrical parameters simultaneously, the factor does not provide a quantitative measure of each damage mechanism.

Theoretical values of n when the I_{SRG} component is dominant are $1 \leq n \leq 2$. Typtical values of n observed for I_{SRG} in this program were $1.5 \leq n \leq 2$. When I_{CH} is the dominant component, $n > 2$. n values were used extensively in this program to identify the I_{CH} component qualitatively because the changes were large and easily detectable. The slope constant must be used with care however, because it is not precise.

The damage mechanisms are easily identified in Figure 3-2 by the slopes of the excess base current ΔI_B curves as a function of V_{BE}. Curve 1 of the figure shows a characteristic dominated by I_{CH}, easily identifiable because $n > 3.7$. Curve 2 shows a characteristic with $n = 2$, which implies that I_{SRG} is the dominant component. Observe that for

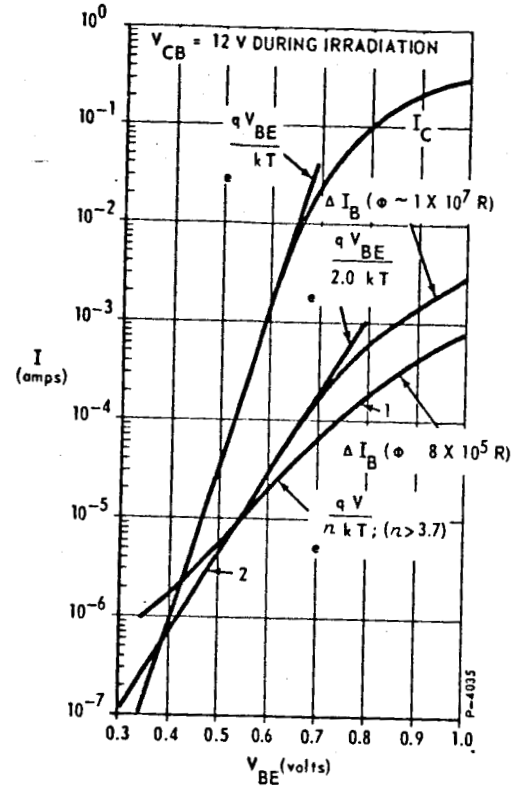


Figure 3-2 - Gain degradation produced by a reverse-biased collector base junction during irradiation

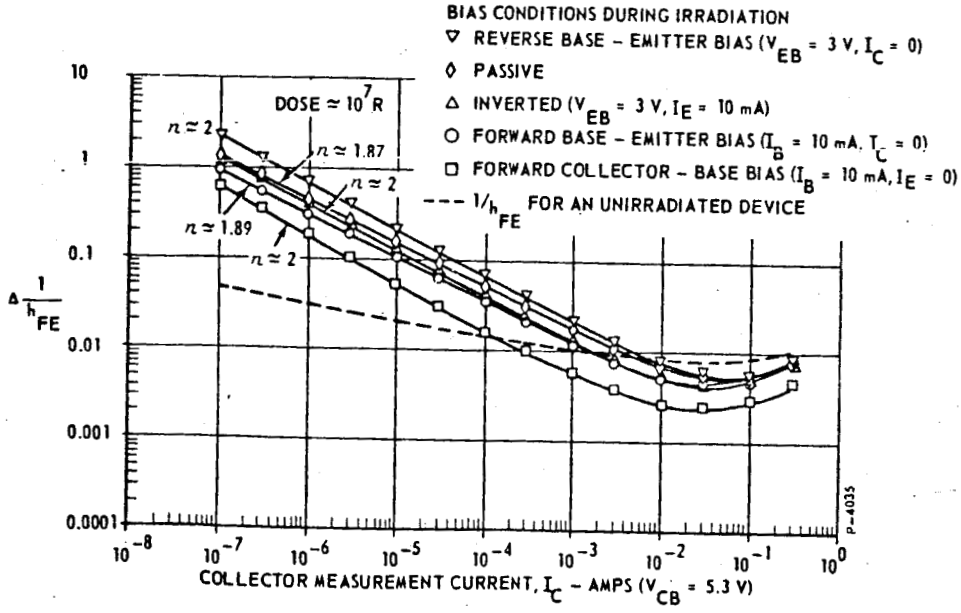


Figure 3-3 – Effect of bias on current gain degradation characteristics

normal bulk diffusion, equation (3.4) still applies and $n = 1$. The curve for I_C in Figure 3-2 shows this relationship. At high injection levels, surface base current effects are apparent in the upward swinging hook shape of the $\Delta \frac{1}{h_{FE}}$ vs I_C characteristic in Figure 3-3.

3.4 EXPERIMENTAL DETECTION OF THE DOMINANT DAMAGE MECHANISMS

The amount of h_{FE} degradation attributed to ionizing radiation induced surface effects is readily determined from the difference in $1/h_{FE}$ prior to and following a dose of radiation. The change in reciprocal gain, hence damage, due to radiation is

$$\Delta \frac{1}{h_{FE}} = \frac{1}{h_{FE}(\phi)} - \frac{1}{h_{FEO}} \tag{3.5}$$

where

h_{FEO} = initial value of h_{FE}, and

$h_{FE}(\phi)$ = value of h_{FE} after dose ϕ.

As mentioned in Section 2.3.2, the low level h_{FE} tester used in this program maintains constant measurement current I_C, subtracts I_{CBO}, and displays values of $1/h_{FE}$ directly. The amount of damage $\Delta \frac{1}{h_{FE}}$ is then readily obtained from a hand or computer subtraction of post and pre irradiation values of $1/h_{FE}$. (Refer to Section 6.2.1.)

Detection of the dominant damage mechanism by experimental methods is accomplished by plotting $\Delta \frac{1}{h_{FE}}$ as a function of I_C to obtain the slope constant n. Mathematical and empirical studies[3.2] have indicated that

$$\Delta \frac{I_B}{I_C} = \Delta \frac{1}{h_{FE}} = K I_C^{\left(\frac{1}{n} - 1\right)} \tag{3.6}$$

The $\Delta \frac{1}{h_{FE}}$ vs I_C characteristic plots linearly on logarithmic paper over almost five decades as shown in Figure 3-3; hence $\left(\frac{1}{n} - 1\right)$ may be taken directly from the plot as the slope of the linear portion of the characteristic. To reduce the large volume of data obtained in the experiment, values of n were calculated by a digital computer program that fitted a

straight line to the linear portion of the $\Delta \frac{1}{h_{FE}}$ vs I_C data by the method of least squares approximation for each increment of damage being investigated. n values were then computed by equating the slope of the computed lines to the exponent in equation (3.6).

I_{CBO} changes were obtained by straightforward leakage current measurements. Techniques for determining the dominant mechanism were not available as in the case of h_{FE} degradation. Catastrophic leakage was not observed in the SiO_2 passivated transistors as has been reported for nonpassivated transistors subjected to ionizing radiation.

In Section 3.1, it is shown that when the charge buildup in the surface oxide is sufficient to cause inversion of bulk material with a subsequent extension of a junction, the junction capacitance increases due to the increased surface area and decreased space charge width. In some transistors, notably the 2N1613, junction capacitance changes were very large and were very good channel indicators. Collector-base capacitance was frequently observed to increase by 100%, from approximately 50 to 100pF, and emitter-base capacitance to increase by 20%, from approximately 62 to 75pF, when transistors were subjected to ionizing radiation with a reverse bias across the collector-base junction. n values during these capacitance excursions were greater than 2, indicating that channels existed. In some transistors, capacitance changes during channel formation were too small to measure accurately with the available impedance bridge. Thus, capacitance increases are good indicators of channel buildup, but the converse is not always true, i.e., a channel is not always accompanied by a measurable increase of junction capacitance.

SECTION 4

RADIATION INDUCED DAMAGE AND STRESS RELATIONSIPS

As discussed in prior sections, electrical parameters of transistors are degraded by exposure to an ionizing radiation field. The radiation itself is a stress on the transistor and the transistor's physical and electrical properties change as a result of the stress. Additional stresses in the form of various electrical biases and/or different ambient media applied to the transistor in conjunction with the irradiation cause damage to build up at differing rates, with different damage mechanisms dominating. These stress combinations of electrical bias and radiation are referred to as bias-radiation stresses. Relationships between these stresses and the resulting damage are presented in this section.

4.1 RECOVERY

Damage removal, or device recovery, was studied as part of the investigation of damage as a function of applied stress. Recovery of irradiated devices to their initial conditions permits testing single devices under a variety of stress conditions, thereby eliminating any influence on the comparative results by variations among devices. Attempts were made to recover irradiated 2N1613 test transistors to their initial conditions using bias-radiation, bias-radiation-temperature, and high temperature stresses. Table 4-1 summarizes the stresses used and the results of the recovery experiments. Combinations of radiation and bias stress (items 1 and 2 of Table 4-1) apparently caused the transistors to return to their preirradiation conditions as indicated by reductions of h_{FE} and I_{CBO} to preirradiation values. However, reirradiation of transistors recovered by these techniques induced damage buildup at rates different from the original damage buildup rates. The damage buildup rate increased in transistors with reverse biased junctions and decreased in transistors with no bias and forward biased junctions. This damage "memory" indicates that the transistors were not fully recovered, that the effects of ionization were not fully equilibrated during the recovery attempts.

High temperature stress proved to be effective in returning 2N1613 transistors (items 3 and 4 of Table 4-1) to preirradiation conditions. This was substantiated by reirradiating 2N1613 devices at the same conditions and comparing damage response as a function of dose. That the rate of damage removal is a function of prior bias-radiation stress history is shown in Figure 4-1. Low level h_{FE} damage (damage measured at low levels of collector current is more stable when induced with an active bias during irradiation. Damage induced in devices having reverse-biased junctions during irradiation is more unstable than damage induced in transistors irradiated passively or with forward biased junctions only. Forward-biased junctions in ionizing radiation induce the most stable surface damage.

Table 4-1 - Recovery experiments

	Recovery Stress	Time (hrs)	Results
1	(a) X ray (5×10^5 R/hr) Forward biased emitter-base, I_C = 100 mA	24	Apparent recovery to initial conditions; damage repeatability poor on reirradiation. Recovery not complete
	(b) Forward biased emitter-base, I_C = 100 mA	24	
2	(a) X ray, Forward biased emitter and collector, I_E = 100 mA, I_C = 100 mA	24	Apparent recovery; repeatability fair to good on reirradiation
	(b) Forward biased emitter and collector, I_E = 100 mA, I_C = 100 mA	24	
	(c) 270°C bake (accelerated aging)	3	
3	Temperature recovery-step stress, details of time and temperatures shown in Figure 4-1		Repeatability excellent Complete recovery
4	Temperature recovery: 320°C. Alternate periods of bias-X ray stress of 10 hours to induce damage and temperature recovery periods	15 5 1/2 63 1/12 1/60	Complete recovery; Repeatability excellent on reirradiation after temperature stresses of 5 hours

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Experiments showed that the more unstable damage induced by reverse bias-radiation stresses could be completely annealed by 300°C stress for one-half hour; however, other bias-radiation conditions induced damage that required up to five hours at this temperature for complete recovery. Stressing all of the transistors at 300 to 320 °C for a period of five hours had no apparent detrimental effects and proved very effective in removing X-ray induced damage from all SiO_2 passivated planar devices tested and in producing h_{FE} and I_{CBO} characteristics equal to or better than those prior to irradiation.

This high temperature stress was used for device recovery in the series experiments of Phase I and in all Phase II experiments.

Ionizing radiation apparently sets up conditions that are non-equilibrium in nature under normal circumstances. When the radiation source is removed, the transistor seeks its preirradiation equilibrium

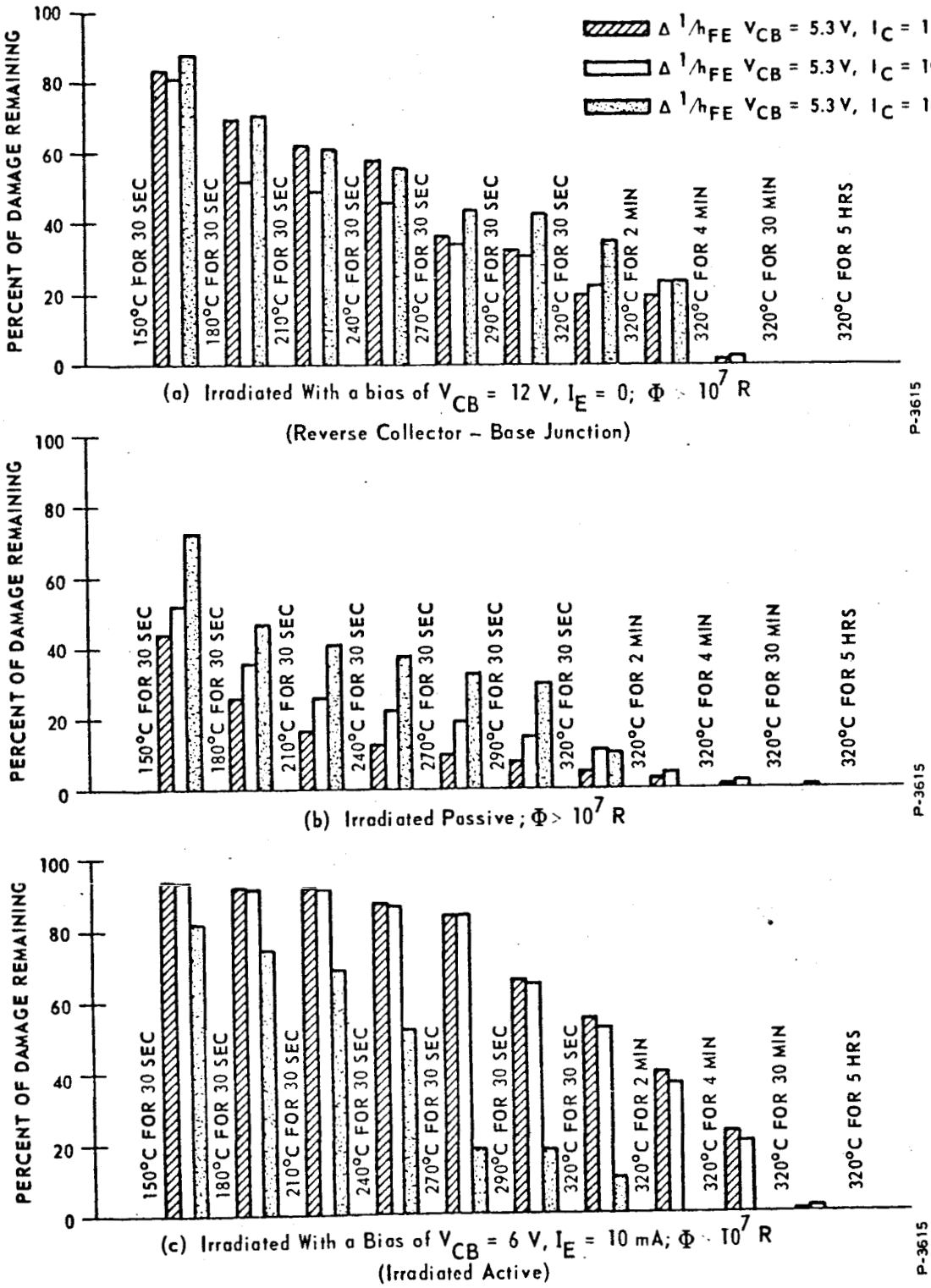


Figure 4-1 – Effect of temperature stress damage on h_{FE} removal

conditions. This is evidenced by shelf-life annealing which, in one investigation produced an average of 20% recovery in 14 transistors in 200 days.[4.1] High temperature stress accelerates recovery by producing conditions near the silicon-silicon dioxide interface that allow faster equilibrium.

Phase II data obtained from mesa and alloy junction devices indicate that the high temperature recovery is evidently not effective for non-planar transistors; in fact, some of these transistors were degraded further by the bake.

4.2 BIAS EFFECTS ON RADIATION DAMAGE

Figure 4-2 shows typical h_{FE} damage characteristics for a single 2N1613 transistor subjected to a series experiment of seven cycles of bias-radiation and recovery stresses. Series testing was used to avoid problems associated with differences in device sensitivity to stress. The seven bias conditions investigated were:

(1) passive

(2) V_{CB} = +12V

(3) V_{CB} = +6V

(4) V_{CB} = +50V

(5) Active: V_{CB} = +6V, I_E = 10mA

(6) Saturation: I_C = 10mA, I_B = 2mA

(7) V_{EB} = +3V

Each bias-radiation condition was followed by a recovery period prior to the subsequent bias-radiation period.

The measurement current selected for demonstration purposes was 100μA because the damage, which is measurement-current sensitive, is sufficiently pronounced to be studied at that current. (See Section 4.3) The 100μA current level is within the linear portion of the damage characteristic, as shown in Figure 3-3, and is well suited to display dominant low level damage mechanism components (either I_{CH} or I_{SRG}).

Figure 4-2 illustrates that reverse bias on either junction during irradiation results in greater total damage than forward bias only (saturation condition) or no bias (passive condition). Also buildup of damage at low doses is more rapid in devices with reverse-biased junctions, with the more gradual damage buildup in transistors with forward bias or no bias. The strong effect of a reverse-biased collector-base junction can be seen from a comparison of the saturation and active bias responses with the same emitter-base forward bias. When the collector-base junction is reverse-biased, damage buildup is considerably greater than for the passive (no bias) case; and when the collector-base junction is forward-biased, the damage is less than for the passive case.

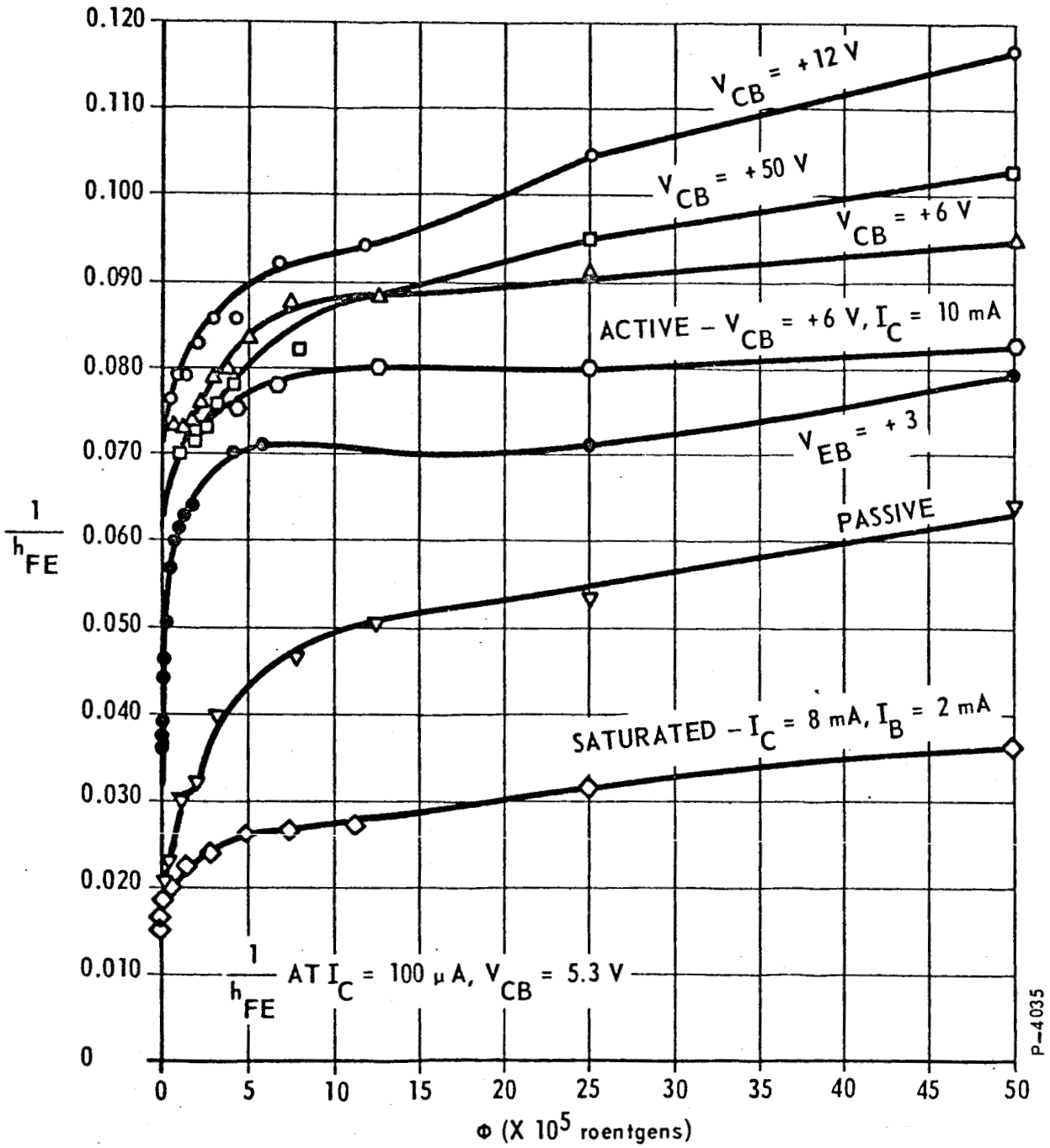


Figure 4-2 - Effects of bias during irradiation on low current h_{FE} damage buildup characteristics for Fairchild 2N1613 transistor 8

The active bias characteristic, i.e., gain damage with the emitter-base junction forward-biased and the collector-base junction reverse-biased (normal amplifier mode), shows that at low doses reverse bias on the collector base junction dominates in damage buildup and that at higher doses the forward biased emitter-base junction attenuates damage buildup. This may be seen by comparing the response for V_{CB} = +6V with the response for active bias and noting that the two responses track closely at low doses and separate as dose increases. Note also that the collector-base junctions had the same reverse bias in both cases.

h_{FE} is primarily dependent upon properties of the emitter and base regions and their junction. The fact that reverse bias on the collector-base junction causes the most significant h_{FE} degradation imples that conditions external to the wafer affect the degradation because there is no apparent internal process by which the collector-base bias can affect the emitter-base junction. This supports the theory that electric fields in the gas ambient surrounding the transistor cause ions produced by radiation to accumulate on the surface of the oxide and thus build up a positive charge over the base and emitter regions resulting in depletion of the p-type region. The larger the fields in the ambient gas, the greater the positive charge buildup on the oxide surface and hence the greater the magnitude of damage buildup. It should be noted, however, that larger reverse biases on the collector-base (+50V) resulted in a smaller magnitude of damage than less bias (+12V). A possible explanation for this seeming paradox is included in the discussion of the model in Section 5.

I_{CBO} damage buildup characteristics as functions of bias during irradiation are shown in Figure 4-3. I_{CBO} damage buildup dependency is similar to that of h_{FE} degradation. However, reverse bias on the emitter-base junction is not as effective in producing I_{CBO} degradation as reverse collector base bias in producing h_{FE} degradation.

Figure 4-4 shows a comparison of changes in junction capacitance and the associated degradation of h_{FE} and I_{CBO} for three different bias conditions during irradiation. The capacitance increases shown in the figure can be interpreted as the introduction of a junction channel. In Figure 4-4(a) for the passive irradiation, h_{FE} degradation gradually increases and capacitance C_{EB} remains constant with dose. In Figure 4-4(b), the rapid h_{FE} degradation with dose is accompanied by an increase of C_{EB} for the reverse collector-base bias during irradiation. This effect can also be observed in Figure 4-4(c) but to a lesser extent due to the forward biased emitter. In the same manner, I_{CBO} builds up gradually and C_{CB} remains constant with dose in the passive irradiation as shown in Figure 4-4(a). A much more rapid increase in I_{CBO} is accompanied by rapidly increasing C_{CB} with dose as shown in Figure 4-4(b). Thus it can be observed that junction capacitances that increase (implying channels) are accompanied by more rapid increases in h_{FE} and I_{CBO} damage than junction capacitances that remain constant. Furthermore, experimental results show that the changes in C_{CB} and C_{EB} occur as a result of reverse bias

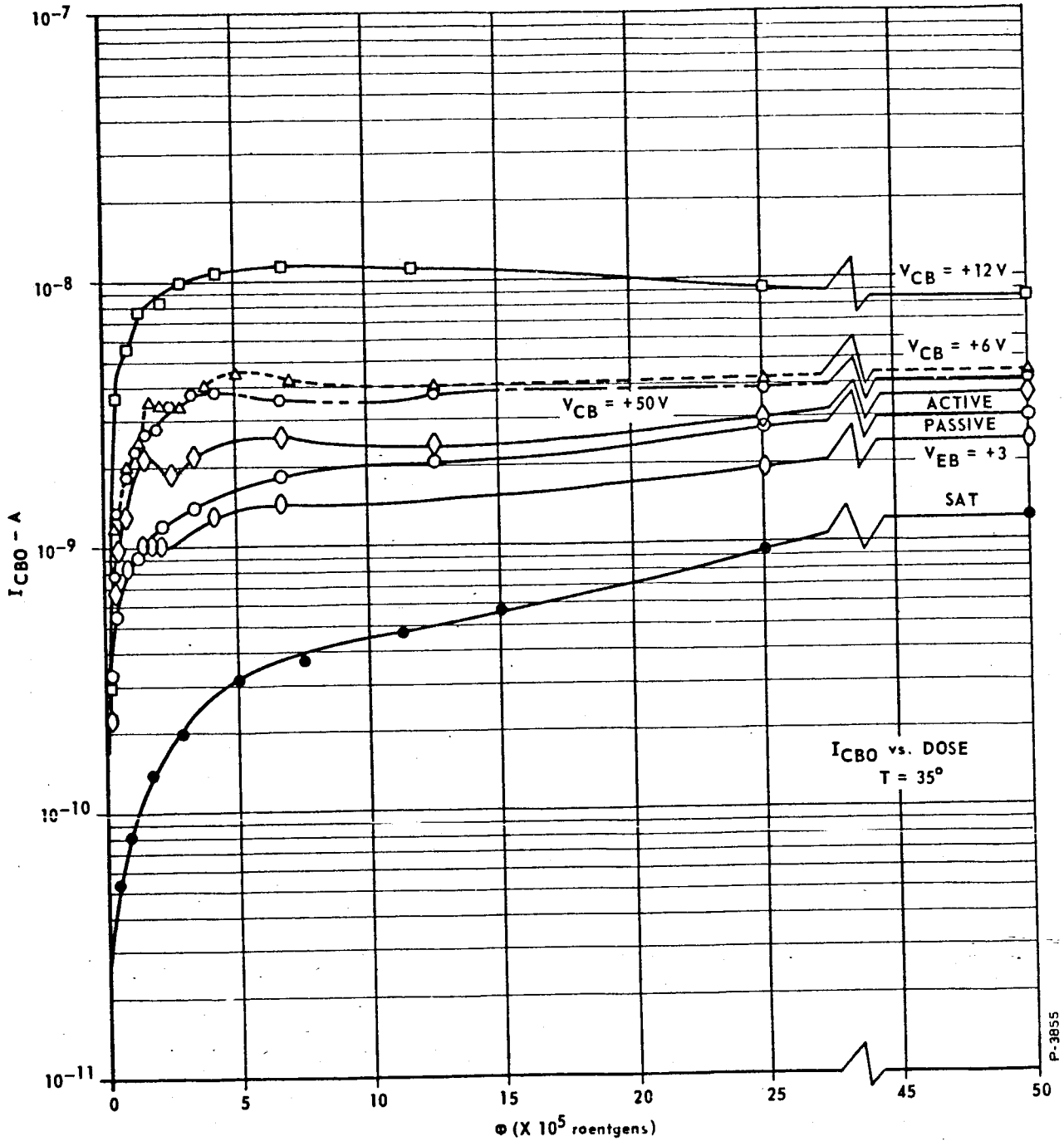
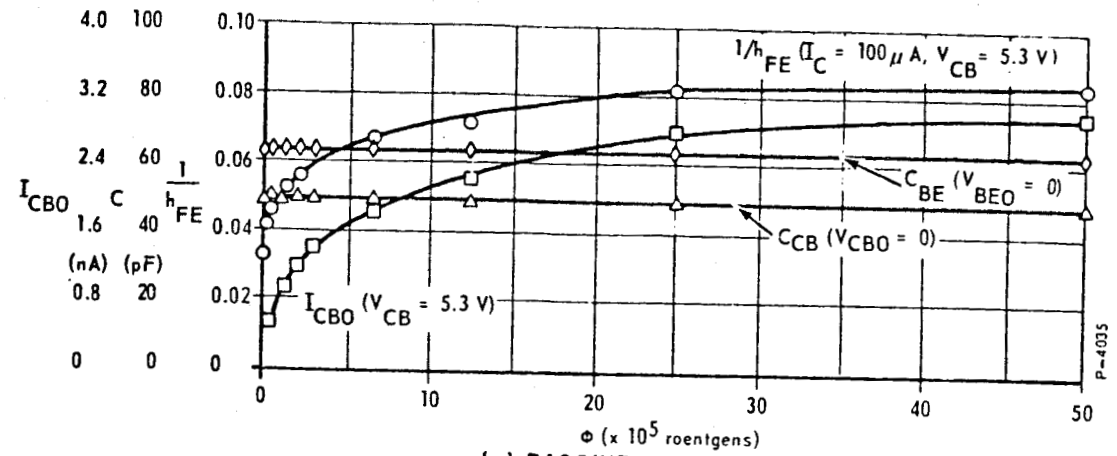
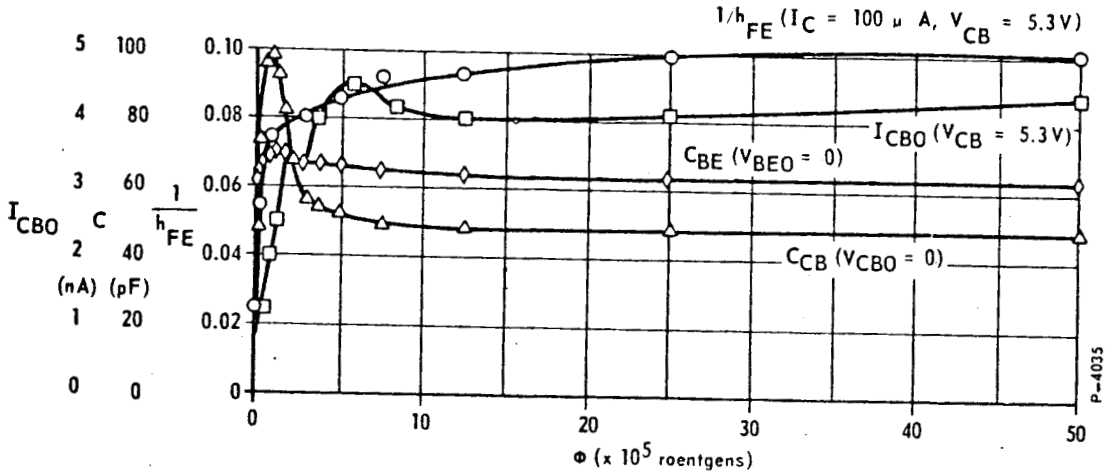


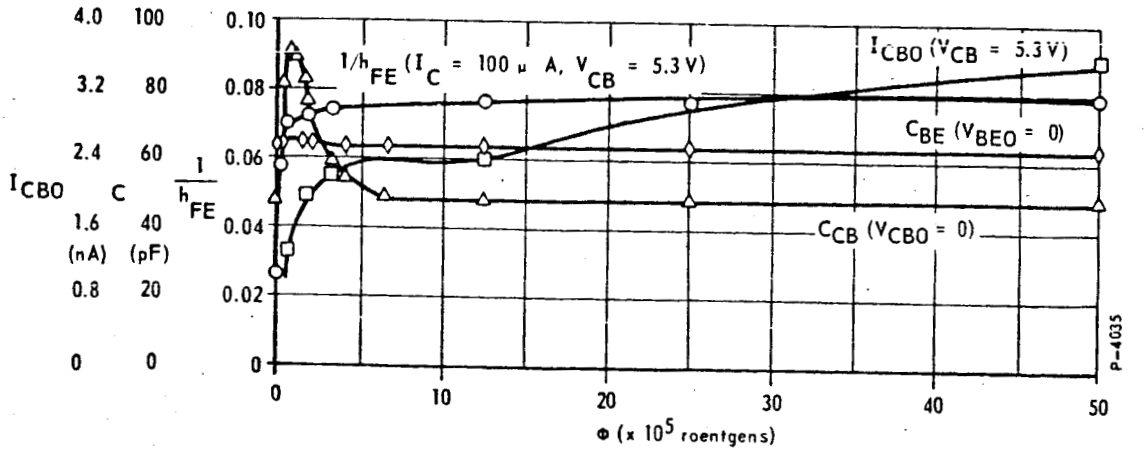
Figure 4-3 - Effects of bias during irradiation on I_{CBO} buildup for 2N1613 transistor 15



(a) PASSIVE



(b) V_{CB} = 6V



(c) V_{CB} = 6V, I_C = 10mA

Figure 4-4 - $1/h_{FE}$, I_{CBO} and junction capacitances as functions of dose for various conditions during irradiation for 2N1613 transistor 15

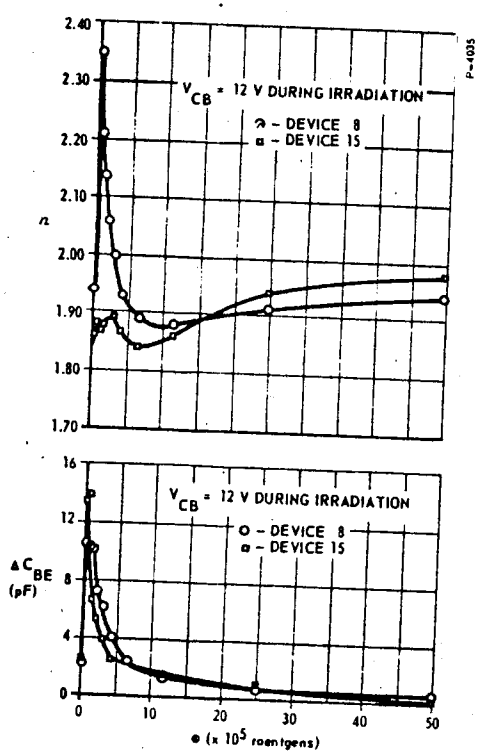
on the collector-base junction. Junction capacitance curves in Figure 4-4(b) and (c) imply that the reverse-biased collector-base junction yields early (low dose) channel components that decay; this is implied by the early peak in the characteristics. This phenomenon, called channel recession, is characteristic of planar SiO_2 passivated n-p-n transistors, but not of p-n-p transistors. (See Section 6.2.2).

Figure 4-5 shows how the existence of a channel in the emitter-base junction was detected from changes in junction capacitance. Note particularly that even though channels apparently existed in both transistors 8 and 15, as evidenced by the increased junction capacitance (reflecting increased junction geometry), the n values indicate that the I_{CH} mechanism was dominant only in device 8; the shape of the n characteristics for device 15 implies that a low dose channel component existed but was not dominant. This demonstrates the limitation of using n alone to detect channels. The capacitance increases show that a channel existed but I_{CH} is dominant only for $n > 2$; hence n is a positive channel indicator only when I_{CH} is dominant.

Increases of I_{CBO} can result from either I_{CH} or I_{SRG}. I_{CBO} was easily measured but there was no apparent experimental technique using the I_{CBO} measurement alone to demonstrate the dominant mechanism, as in the case of h_{FE} degradation. C_{BC} measurements provided a means for identifying a collector base channel in some devices. Figure 4-6 shows how capacitance values reflect the existance of channels in the collector-base junction. I_{CBO} at low doses, when a channel exists, peaks two decades greater in transistor 8 than in transistor 15, indicating poorer surface interface structure with more generation sites in transistor 8.

4.3 EFFECTS OF MEASUREMENT CONDITIONS

Results of the experiments performed by irradiating 2N1613 transistors and measuring the damage at different current levels revealed that rate and magnitude of h_{FE} damage buildup is dependent upon measurement conditions, with different damage components dominating at different injection levels. Figure 4-7 illustrates this dependence vividly. Damage buildup is considerably greater and more rapid at low currents than at higher currents. The rapid rise is attributed to I_{CH}, which dominates at low injection levels and diminishes at higher injection levels. I_{SRG} also is most effective at low levels. Both I_{CH} and I_{SRG} decrease in value to negligible quantities as injection level is increased. Also, as injection level is increased, an effect known as base spreading occurs, in which the relatively large base current produces a voltage gradient across the base region. This causes the base-emitter junction near the surface to have a larger forward bias voltage than the bulk junction, diminishing emitter efficiency and increasing recombination velocity characteristics of the surface. A combination of the low and high level effects yields damage as shown in Figure 3-3 where the linear decrease in damage at low levels is due to an I_{SRG} component and the dish-up at high levels is due to the base spreading effect.



(a) EXPONENTIAL SLOPE CONSTANT

(b) CHANGE IN C_{BE}

Figure 4-5 - Exponential slope constant and base emitter capacitance as functions of dose for 2N1613 transistors 8 and 15

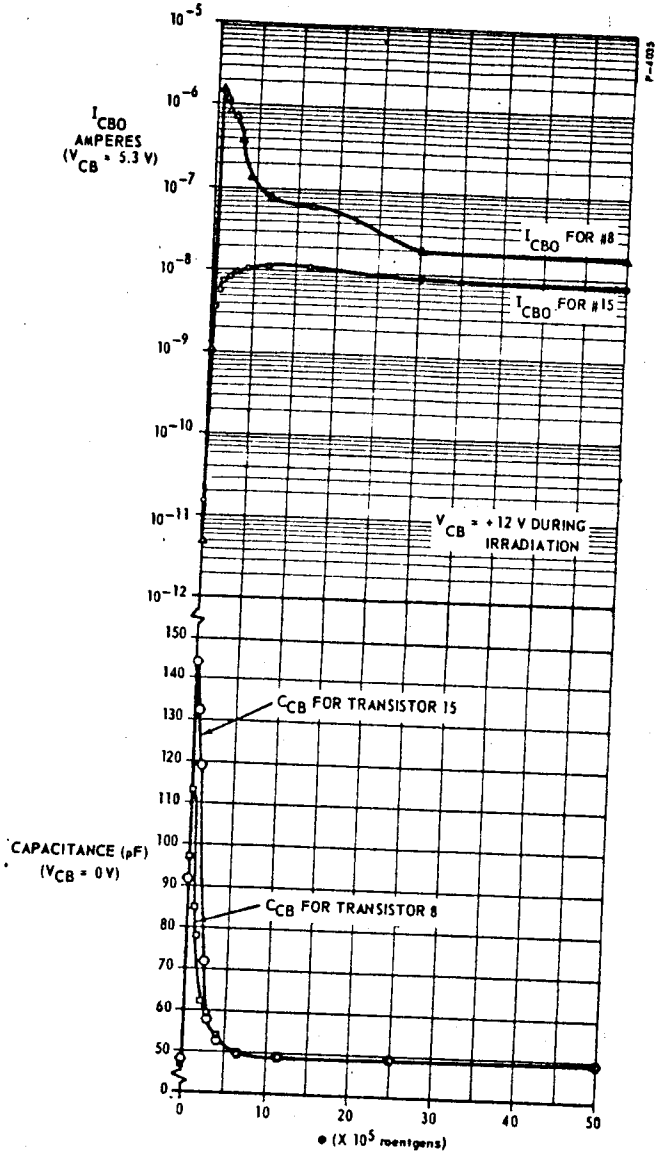


Figure 4-6 - I_{CBO} and C_{CB} as functions of dose for 2N1613 transistors 8 and 15

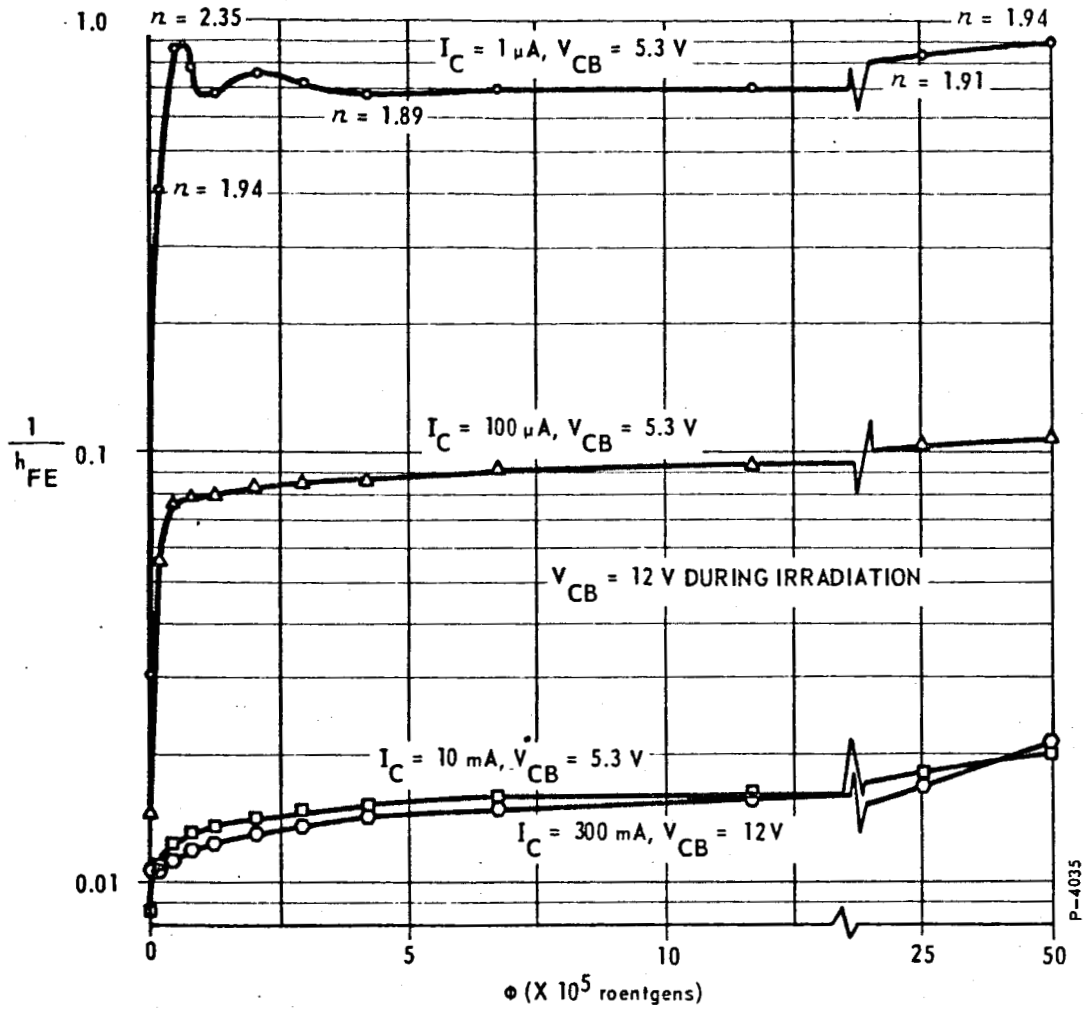


Figure 4-7 - Current gain versus dose at different measuring currents for 2N1613 transistor 8

4.4 EFFECTS OF AMBIENT MEDIA

All of the effects discussed so far in this report are attributes of damage the transistor incurs in its normal ambient medium (usually dry nitrogen or air). To determine the effects of dry nitrogen on damage characteristics, eight 2N1613 transistors having various radiation histories were recovered and placed in glass envelopes (shown in Figure 4-8) which were evacuated to about 10^{-8} Torr. The transistors were then irradiated with various electrical biases.

Damage buildup for forward-biased and passive transistors irradiated in the vacuum appeared to be similar to those produced in their normal ambient media, implying that the I_{SRG} damage component is independent of the ambient medium of the wafer.

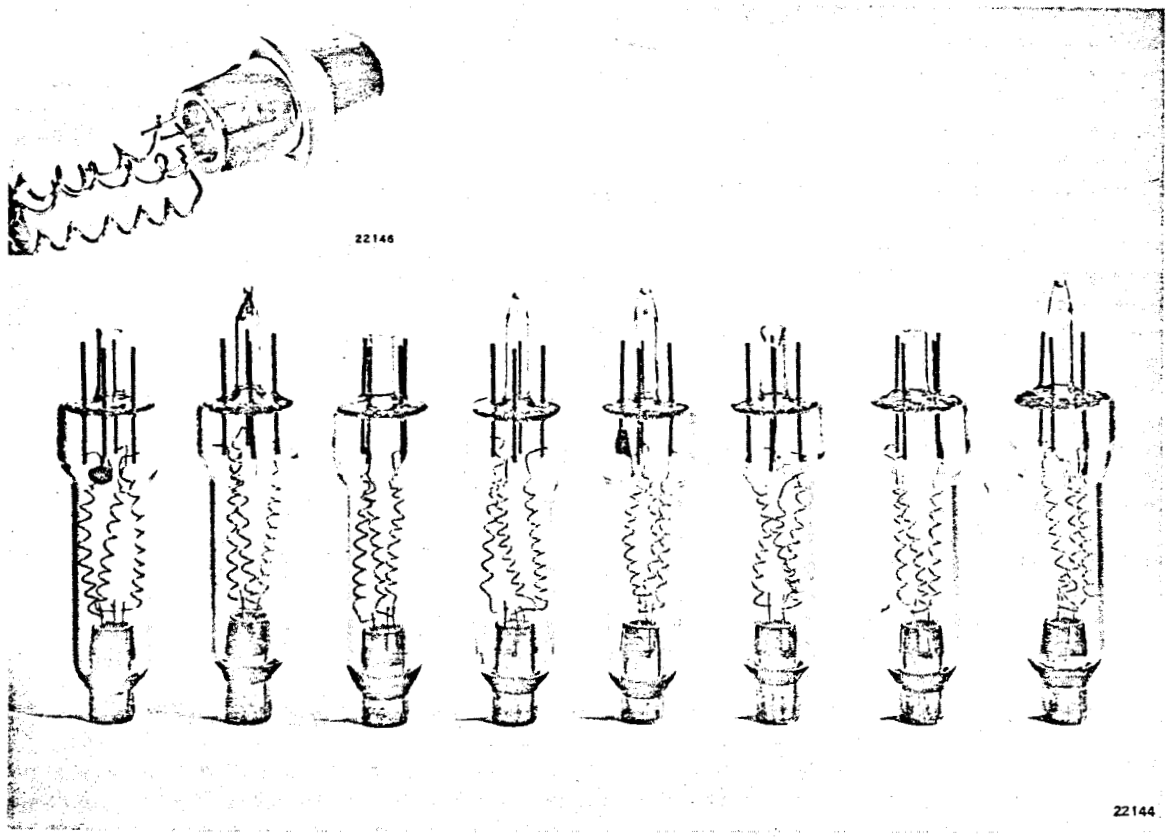


Figure 4-8 - Ultrahigh vacuum envelopes for irradiating transistors

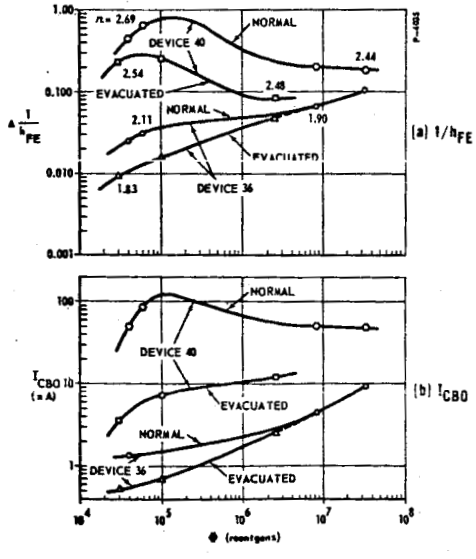


Figure 4-9 - $1/h_{FE}$ and I_{CBO} versus dose for normal and evacuated ambient media for 2N1613 transistors 36 and 40

To amplify the effects of reverse bias conditions in a vacuum, one transistor with relatively good tolerance and another that was extremely sensitive to radiation were recovered and subjected to bias-radiation stresses in vacuum. Figure 4-9 shows that removing the ambient gas decreased the early h_{FE} and I_{CBO} damage buildup in both devices. For transistor 36, the damage response curves become asymptotic at large doses, indicating that only the early damage attributed to channeling is reduced by vacuum.

Hogrefe[4.2] reported on an irradiation-vacuum test accomplished by piercing the encapsulating cans of type 2N1711 (a high gain 2N1613) transistors aboard an experimental payload prior to placing them in orbit in the Van Allen belts. Evacuated and normal devices were in space radiation for 100 days ($\sim 10^5$R) with an active bias of V_{CE} = 10V, I_C = 0.5mA. Due to solar cell degradation, this bias had to be removed after 100 days, so that the devices were passive during irradiation for the remainder of the mission. Hogrefe reports that during the first 100 days evacuated units exhibited much less damage than normally encapsulated units,[4.2] while after several hundred days[4.3] of passive irradiation the difference in damage between vacuum and gas ambient no longer existed. These data are in basic agreement with those observed for X-rays, where vacuum reduced the early channel component in devices with a reverse collector-base but had little influence on devices irradiated passively.

Following several radiation and recovery stress cycles in vacuum, some of the transistors were subjected to bias-radiation stress in air. Damage buildup in air, although greater than damage induced in a vacuum, was less than the damage induced in the normal transistor ambient medium. The reason for this unexpected result is unknown.

4.5 EFFECTS OF DOSE RATE

Series testing of several 2N1613 transistors at 5 x 10^5R/hr, 5 x 10^4R/hr, and 5 x 10^3R/hr indicated that damage buildup is affected by dose rate. No conclusions could be drawn, however, because of the inconsistency of the effects.[4.4] A reverse collector-base bias of +50V was used during the rate tests. The effects of this extreme bias may have masked the dose rate effects by inverting the p material beneath the base without requiring charge migration through the oxide. This phenomenon is discussed in Section 5.

4.6 EFFECTS OF TEMPERATURE DURING MEASUREMENT

An investigation was made to determine the magnitude of the damage temperature coefficient, if any. The temperature was varied during measurement of h_{FE} damage in 2N1613 transistors irradiated under various bias conditions. Results show that the temperature coefficient of damage is a function of the measuring current, the bias used during irradiation, and the dose. Figure 4-19 shows the temperature coefficient of damage as a function of collector current in transistor 8 before irradiation and after several series tests with various biases and doses. Figure 4-11

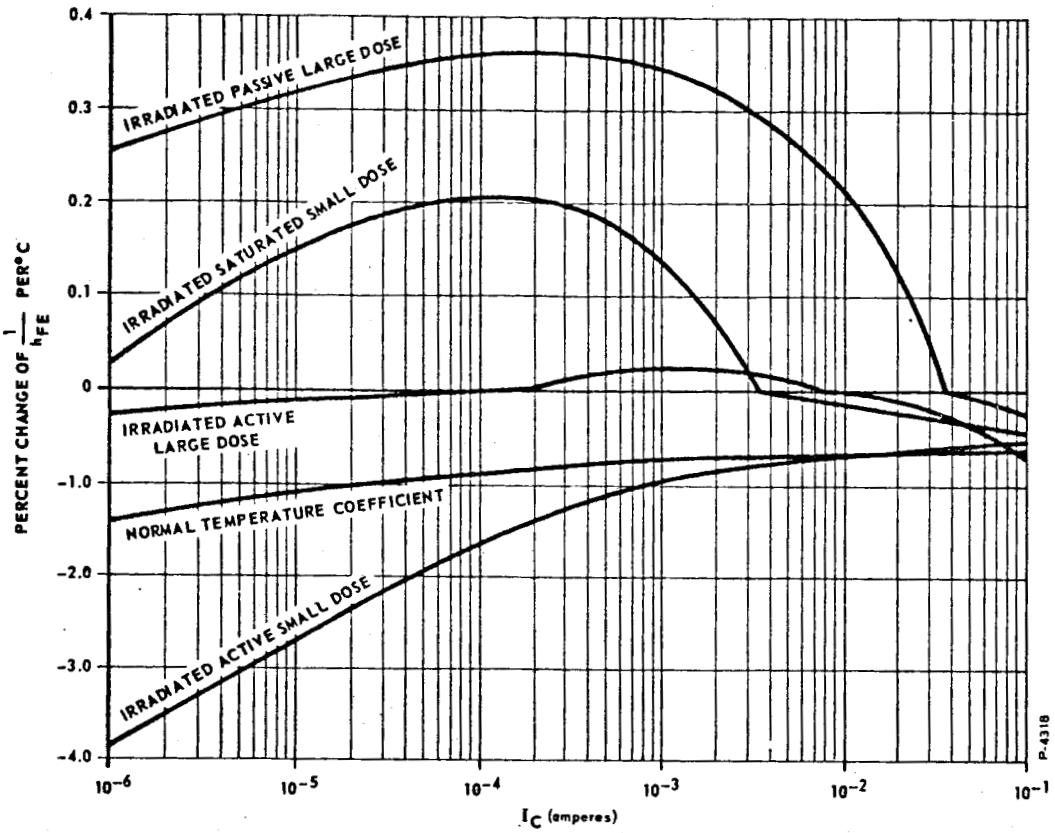


Figure 4-10 - Temperature coefficient of h_{FE} degradation for 2N1613 transistor 8

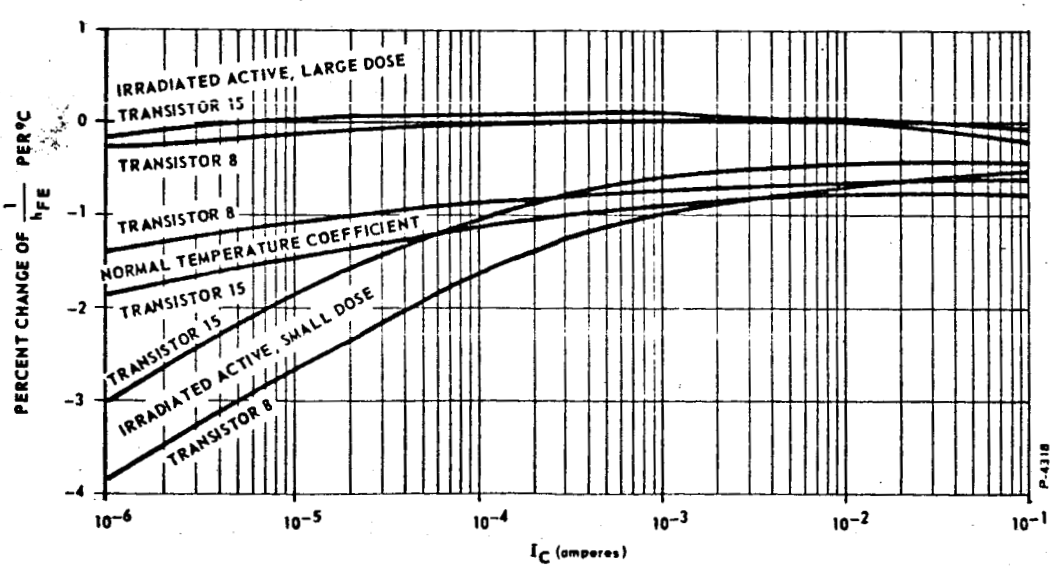


Figure 4-11 - Temperature coefficient of h_{FE} degradation, comparison of 2N1613 transistors 8 and 15

gives a comparison of the temperature coefficient of damage for transistors 8 and 15 before irradiation and after irradiation at low and high doses in an active mode. Note that after small doses the temperature coefficient for active devices increases significantly and is extremely sensitive to collector current, whereas after large doses, it decreases significantly.

4.7 COMPARISON OF TEMPERATURE AND IONIZING RADIATION INDUCED DAMAGE

Damage was induced in 2N1613 transistors using various high temperature-bias stresses for the purpose of comparing high-temperature and ionizing-radiation induced damage. Reverse biases were used since they produce the largest amounts of damage in irradiated transistors. Temperature stress induced very little damage in the transistors until they were reverse-biased to breakdown; the damage induced then was permanent, unlike the easily annealed ionizing-radiation-induced damage. No correlation could be made between the temperature and radiation induced damage, however, because the amount of annealable damage produced by the reverse-bias high temperature stress was insignificant.

SECTION 5

DAMAGE MODEL

The foregoing results, which constituted Phase I of the program, were sufficient for developing theories concerning the nature of damage build-up. These theories are presented in the form of a damage model.

The first model to explain leakage current and gain changes in bipolar transistors was proposed by Peck et al[5.1] based on studies of exposure to ionizing radiation of silicon mesa transistors which were not SiO_2 passivated. h_{FE} and I_{CBO} degradation, according to this model are due to surface channels produced by an accumulation of charged ambient gas ions on the device surface. These gas ions are attracted to the transistor surfaces by electric fields produced when the device is electrically biased. A more recent investigation[5.2] modifies this model for SiO_2 passivated devices, suggesting that actual deposition of gas ions on the oxide surface does not occur, but that instead ions traveling very close to the surface give up their charge to oxide surface "sites."

Several investigations[5.3, 5.4, 5.5, 5.6] of ionizing radiation effects on MOS structures have shown the existence of a second mechanism for surface degradation--migration of charged species in the SiO_2 insulating layer when an electric field is applied across the oxide layer. Either of these mechanisms results in an accumulation of space charge over silicon, altering the surface potential of the semiconductor. This change in silicon surface properties is usually manifested by enhancement, depletion or inversion of surfaces, changes in surface recombination velocity, and changes in p-n junction characteristics.

Investigators hold opposing views as to which of the above mechanisms dominates for silicon planar bipolar transistors. Hughes[5.7] concludes, from Co-60 irradiations of normal and evacuated 2N2801 p-n-p transistors, that ionizing radiation surface effects occur as a result of drift of mobile space charge in the SiO_2 layer and not as a result of conditions external to the wafer. Stanley[5.8] concurs with this conclusion. Hogrefe[4.2] reports that normal 2N1711 n-p-n planar transistors irradiated in the Van Allen belts suffered considerable loss of gain, while devices evacuated by piercing the encapsulating can suffered almost no gain loss after 100 days in orbit ($\sim 10^5$R). He concludes that gas ionization is a cause of these surface effects for planar transistors. Phase I of this investigation has shown that proper choice of dose, bias during irradiation, and measurement conditions could lead to either of these conclusions.

The following discussion of the model considers two categories of bias conditions during irradiation: one with passive or forward-biased junctions, which produce no electric fields in the gas ambient; and the second with a reverse bias on at least one of the device junctions, which produces significant electric fields in the gas ambient.

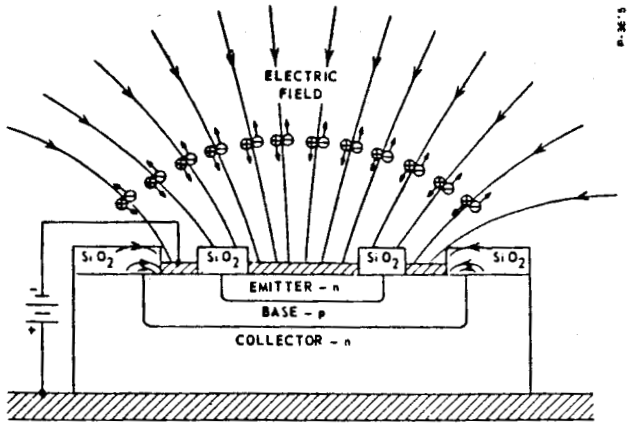
5.1 PASSIVE OR FORWARD BIAS DURING IRRADIATION

In the first case, where both junctions are either passive or forward-biased, gas ion collection on the oxide surface is unlikely since the ambient has no significant electric field. Space charge migration can occur, however, in the SiO_2 layer directly over a junction, caused by the fringing field due to the junction transition region potential. The polarity of this potential is such that a positive mobile charge migrates laterally in the oxide toward the p side of the junction, and/or a negative charge migrates toward the n side. This type of space charge buildup reduces the silicon surface potential near the junction, which causes the junction transition region to widen at the SiO_2 interface and the surface recombination velocity to increase. The increases in junction geometry and surface recombination velocity enhance the I_{SRG} component. The high current h_{FE} component is also enhanced by the base region surface recombination velocity and by the injection which occurs near the surface.[3.2] The oxide charge migration and resultant junction widening reduce the junction fringing fields, which decelerates the process and eventually produces a saturation condition. Irradiation tests of passive and forward bias n-p-n devices indicate that this is a slow process and that it does in fact produce damage characteristic of I_{SRG}. Forward bias junctions produce less damage than passive, as expected, since the forward bias reduces the junction transition region voltage, which in turn reduces the fringing field in the oxide.

5.2 REVERSE BIASED COLLECTOR-BASE DURING IRRADIATION

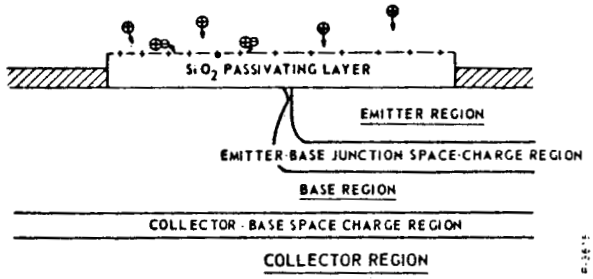
n-p-n transistors irradiated with a reverse bias on the collector-base junction develop an I_{CH} component in base current which increases rapidly during early radiation exposure, accompanied by an increase in C_{BE} and an n in excess of 2. Since the collector-base fringing field is too far from the base-emitter junction to exert a strong influence, the gas ion model is included in the explanation of this behavior. Figure 5-1 depicts the model to be discussed.

A reverse collector-base bias produces an electric field in the gas surrounding the device wafer. For n-p-n transistors this field attracts positively charged gas ions[5.1] to the SiO_2 surface over the base region [See Figure 5-1(a)], and these ions give up their positive charge to SiO_2 surface "sites" by attracting electrons from these sites[5.2] [See Figure 5-1(b)]. This positive space charge over the base region surface can account for the sensitivity of damage to collector-base bias and, if the space charge density is great enough, explain the creation of an inversion layer or channel over the base region. The Fairchild 2N1613 has a base region oxide thickness of from 4000 Å to 6000 Å, and the base surface carrier concentration ranges from 2×10^{18} cm^{-3} to 5×10^{18} cm^{-3}. The potential required across the oxide at the onset of inversion for the above dimensions ranges from 22 volts to 54 volts.[5.9] The voltage across the oxide layer due to gas charging the SiO_2 surface can be no greater



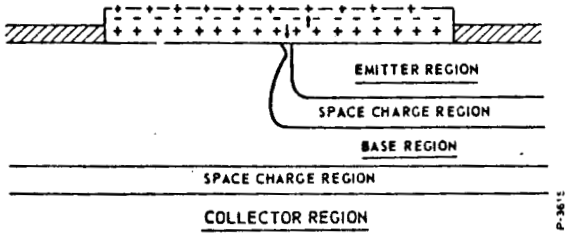
ATTRACTION OF POSITIVE GAS IONS TO BASE AND EMITTER REGIONS BY REVERSE COLLECTOR–BASE BIAS

(a)



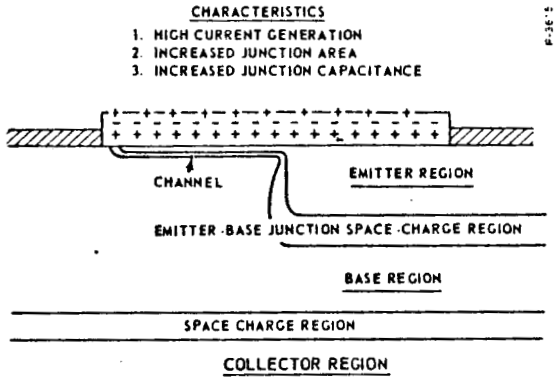
CREATION OF $Si O_2$ SURFACE SPACE CHARGE BY INTERACTION WITH GAS IONS

(b)



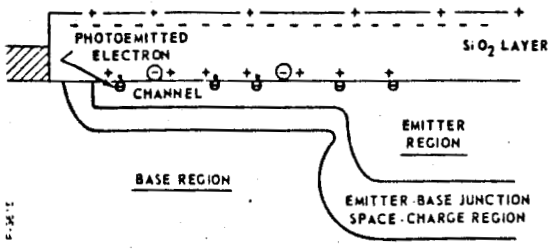
MIGRATION OF IONIZED SPECIES IN THE OXIDE CAUSES A DRIFT OF POSITIVE SPACE CHARGE TOWARD THE INTERFACE

(c)



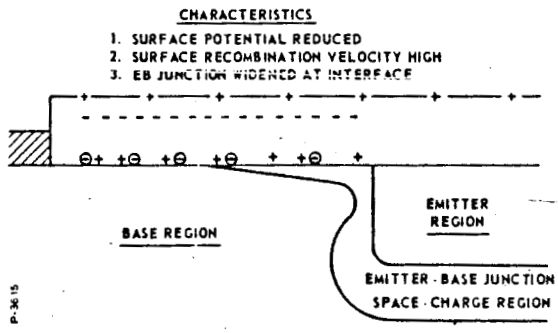
CHANNEL INDUCED BY ACCUMULATION OF POSITIVE SPACE CHARGE AT THE $Si O_2$ –Si INTERFACE

(d)



CANCELLATION OF POSITIVE CHARGE IN SiO_2 LAYER DUE TO PHOTOEMISSION OF ELECTRONS

(e)



RECESSION OF CHANNEL DUE TO CANCELLATION OF POSITIVE OXIDE SPACE CHARGE

(f)

Figure 5-1 - Model of ionizing radiation surface effects

than the voltage applied at the collector-base junction. Since V_{CB} = 6V produces significant channels, space charge migration in the oxide must be included to explain the channel.

Mobile charge species created by ionizing radiation in SiO_2 migrate under the influence of an electric field, as evidenced by the results of ionizing radiation studies of MOS structures. In the case of the MOS device, the electric field is created by the applied gate bias; while in the bipolar transistor, the field is due to an accumulation of oxide surface charge. However, the space charge migration processes within the oxide and the effects on the silicon beneath the SiO_2 are similar for both device types. The migrating charge species, either positively charged, negatively charged, or both, produce a net positive space charge drift toward the SiO_2-Si interface [See Figure 5-1(c)]. This results in an increased electric field in the oxide near the interface and inversion of the p-type base region beneath the interface [See Figure 5-1(d)]. This model is similar to that proposed by Grove and Snow[5.6] for an MOS device, where electron-hole pairs are generated by ionizing radiation. The electrons from these pairs migrate toward the positive side of the oxide leaving holes trapped near the negative side.

Though this positive space charge near the SiO_2-Si interface accounts for channel formation, it cannot explain the observed behavior of n-p-n transistors since it provides no means of removing the channel at large doses. This apparent reduction of positive space charge at large doses suggests a transfer of charge across the SiO_2-Si interface. Photoemission of electrons from silicon across the SiO_2-Si interface, as discussed by Williams,[5.10, 5.11] explains the elimination of base region channels from n-p-n transistors at large doses. The electron threshold energy for photoemission is 4.22eV for a p-type surface and 3.05eV for an n-type surface — energies easily achieved with the ionizing radiation sources of interest. Electrons emitted from the silicon into the SiO_2 cause a net reduction in the positive space charge over the interface [See Figure 5-1(e)]. Photoemission is dependent on the electric field at the SiO_2-Si interface. For n-p-n transistors with reverse biased collector-base junctions during irradiation, the net positive oxide space charge drift to the interface over the p-type base region produces an electric field which enhances the probability of photoemission into the oxide. At some point, the net positive charge drift to the interface equals the net flow of photoemitted electrons to the interface. As photoemission continues, the positive space charge decreases, which in turn reduces the interface electric field and the channel. Eventually the space charge decreases to a point where the channel disappears [See Figure 5-1(f)] and photoemission either ceases or continues at a low rate to replenish electrons crossing the oxide-ambient interface.

The results of irradiating an n channel enhancement MOS device indicated that photoemission does not produce complete recovery to initial conditions but instead raises the surface potential to a large value which then decreases to a smaller value of the same polarity. This may explain the large I_{SRG} component remaining after channel recession in n-p-n

transistors, since the surface charge density is reduced to a value insufficient to invert the high base region surface concentration but sufficient to leave a depleted region. This depleted region enhances I_{SRG} and base spreading components.

SECTION 6

SEMICONDUCTOR DEVICE EVALUATION

6.1 DEVICE SELECTION

The ideal solution to the problems of ionizing radiation surface effects on transistor electrical parameters is to provide that combination of materials, geometry, surface treatments and biases that eliminates or negates the effects. Since such a combination is not presently available, the next best solution is to minimize the effects. Two approaches were taken to achieve transistors with minimum susceptibility to ionizing radiation: (1) evaluation of the surface stability in ionizing radiation of a number of different transistor types currently being produced or in development, and (2) development of a screening process whereby transistors with poor surface stability in ionizing radiation can be identified to preclude their use in radiation environments. This section describes the results of the first approach. Several types of transistors were evaluated for their tolerance to ionizing radiation surface effects. The same transistors were also subjected to the recovery procedure described in Section 4 and irradiated a second time to provide data for evaluating the effectiveness of the screening process that is discussed in detail in Section 7.

A number of devices tested in this phase were selected because they were manufactured with special surface treatments or contained special passivation processes, such as a guard ring or field plate, designed specifically to improve nonradiation surface stability and surface characteristics. The purpose of testing these devices was to determine if any of the special techniques were effective in eliminating or substantially minimizing radiation surface effects.

Other types of transistors were selected to complete the evaluation for different configurations and different geometries: n-p-n vs p-n-p, bipolar vs unipolar (FET) and signal vs power transistors. A complete listing of the devices evaluated and the reasons for their selection are given in Table 6-1.

6.2 RESULTS OF THE EVALUATION

The device evaluation program consisted of irradiating samples (nominally 12, sometimes 6 as listed in Table 6-1) with X-rays at a rate of 5×10^5R/hr with reverse-biased collector-base junctions (the condition inducing the most severe surface effects). Changes in h_{FE} and I_{CBO} were monitored over the full range of collector currents as a function of total dose received. Data for evaluating the effectiveness of screening in these devices were provided by a second irradiation identical to

Table 6-1 - Devices tested in Phase II

	Device No.	Mfr.	Description	Quantity Tested
1	2N1613	Fairchild	n-p-n	12
2	2N2222	Motorola	n-p-n, annular ring process	12
3	2N2222	Fairchild	n-p-n, without annular ring	12
4	2N2905	Motorola	p-n-p, annular ring process	12
5	2N1132	Texas Inst.	p-n-p, TriRel process, field relief plate over collector-base junction	12
6	2N722 2N722	Texas Inst. Motorola	p-n-p, field plate p-n-p, without field plate	6 6
7	STC1739	Silicon Trans. Corp.	n-p-n, Si, 200 W, mesa, structure	12
8	2N2771	Westinghouse	n-p-n, Si, 200 W, alloy junction	12
9	2N3058	Crystalonics	p-n-p, epitaxial mesa collector-base and planar emitter-base construction, Low level, high gain, low V_{sat}	6
10	2N3964	Fairchild	p-n-p, Planar II process	6
11	2N2219A	Motorola	n-p-n, six modified with metallization over emitter-base junction	12
12	TD106	Fairchild	n-p-n, six modified with metal gate electrode over emitter-base junction	12
13	2N3387	Siliconix	JFET, Flat package, ceramic	12
14	2N3609	General Microelectronics	MOSFET, Differential amplifiers	12

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the first performed on the devices after they had been restored to initial conditions by the high temperature recovery cycle described in Section 4-1.

The magnitude and rate of the changes in h_{FE} and I_{CBO} occurring with radiation are indications of the susceptibility of the devices to radiation surface effects. Repeatability of the damage buildup in the second cycle is a measure of the effectiveness of the screening technique.

Experimental results of the evaluation of the different device types are presented below. Figures 6-1 through 6-12 show values of $1/h_{FE}$ and I_{CBO} for a number of devices after both small and large exposures to ionizing radiation. The $1/h_{FE}$ data are for 10^{-4} ampere of collector current except for the power transistors. Power transistor $1/h_{FE}$ data are shown at 10^{-1} ampere.

Straight line plots were made from the two data points for the purpose of comparing the relative sensitivities of various devices to surface effects.

These plots do not provide a complete evaluation of the response of individual devices to ionizing radiation, but time did not permit taking a large number of points on all devices. However, the plots do provide useful data for evaluating relative device sensitivities for two reasons: (1) the shapes of the damage curves are consistent for all devices, i.e., they have a fast buildup at small doses and gradually saturate at higher doses. The low dose, low current point indicates channel formation and its effect on gain and leakage current, while the high dose, low current point indicates surface space charge recombination generation effects. (2) the low dose point represents the optimum value, i.e., near or at the peak of the initial damage buildup. Capacitance measurements which show the formation of a channel were made on several test subjects of each type irradiated and data points were taken when the capacitance reached a peak or leveled off.

Two irradiation cycles are shown on the graphs because the data are also used for evaluating the screening technique. Since the graphs are logarithmic plots of total does, initial values of $1/h_{FE}$ and I_{CBO} prior to each cycle are not shown, but rather are given in tables on each graph.

In addition to the plots of damage vs radiation dose for fixed collector current, there are plots showing damage as a function of collector current at both low and high radiation doses. Rather than representing such data on all devices tested, the plots (Figures 6-13 through 6-32) show the spreads of the changes in $1/h_{FE}$ among all devices of a given type tested. In many of these figures, a broken line characteristic within the spread indicates how screening reduces the spread in damage among devices. The improvements due to screening are discussed in detail in Section 7.

6.2.1 Bipolar n-p-n Transistors

Gain and leakage current degradation as a function of radiation exposure for three typical bipolar n-p-n transistors are shown in the plots of $1/h_{FE}$ and I_{CBO} in Figures 6-1, 6-2, and 6-3. I_{CBO} changes in some devices are quite large, but absolute magnitudes are still very small for most transistors. Typical h_{FE} degradation in n-p-n transistors is characterized by the development of emitter-base and collector-base channels at low doses, which recede after large doses. This effect can be seen in Figures 6-33 and 6-34, which are plots of typical slope constant n as a function of dose for two types of n-p-n transistors. Values of n were computed by digital computer techniques using the data of $1/h_{FE}$ vs I_C, and their magnitudes are not necessarily exact because the computer calculates a best fit without interpreting the meaning of data. The reduction of n with dose is significant because it supports the conclusion that channel recession due to photoemission of electrons across the $Si-SiO_2$ interface, as described in the damage model discussion (Section 5), is common to planar n-p-n transistors.

Channel buildup and recession are manifested in the plots of Figures 6-1, 6-2 and 6-3 by rather large changes in $1/h_{FE}$ at low doses and a leveling off (or sometimes reduction) to saturation values at higher doses. The magnitude of the changes and the variation among the different devices of a type are relatively large for all three types of n-p-n devices at 10^{-4} ampere. These effects are illustrated most prominently by the changes in $1/h_{FE}$ due to radiation independent of the initial value for different levels of collector current. The magnitudes and spreads of the changes are indicative of the surface stability in radiation of a particular transistor type.

Figure 6-13 and 6-14 show the upper and lower values (hence the total spread) of radiation-induced gain damage $\Delta \frac{1}{h_{FE}}$ as a function of collector current for 12 Fairchild 2N1613 transistors for small ($< 10^5$R) and large ($\sim 10^7$R) doses respectively. Both the magnitude and the spread of damage due to radiation decrease with collector current until they reach a minimum, after which they gradually increase. Whereas the spread in $1/h_{FE}$ damage is smaller at high doses than at low doses, the average magnitude of damage is greater at high doses. At 10^{-4} ampere, the spread of $\Delta \frac{1}{h_{FE}}$ is from 0.026 to 0.23 at low doses (4×10^4R). To understand how these changes in $1/h_{FE}$ are reflected in the final gain of a typical 2N1613, consider a transistor with an initial gain of 50 at 10^{-4} ampere (about the average for the devices tested), and, by employing equation (3-5), calculate the final gain as follows:

$$h_{FE1} = \frac{1}{\frac{1}{h_{FEO}} + \Delta \frac{1}{h_{FE}}} = \frac{1}{1/50 + 0.026} \tilde{=} 22$$

$$h_{FE2} = \frac{1}{1/50 + 0.23} \tilde{=} 4$$

Figure 6-38 provides a family of curves that facilitates calculation of h_{FE} after irradiation for any transistor when the amount of gain degradation $\Delta \frac{1}{h_{FE}}$ due to radiation and the initial value of h_{FE} are known. These curves are plots of equation (3-5) relating h_{FE} to gain degradation for various initial values of h_{FE}. Thus, to graphically find the h_{FE} values calculated above, locate the value of $\Delta \frac{1}{h_{FE}}$, i.e., 0.026, on the abscissa in Figure 6-38 and read off the post radiation value of h_{FE} on the ordinate at the intersection of the 0.026 line and the curve for the initial h_{FE} value of 50. The above example is shown

also on the nomograph, Figure 6-39, which is more complete because it is not restricted to only five values of initial h_{FE}. The curves of Figure 6-38 demonstrate that for large values of damage, post radiation h_{FE} values are almost independent of initial gain, which can be ignored when only approximate results are required.

At a large dose (3.5×10^7R), the spread of $\Delta \frac{1}{h_{FE}}$ is from 0.09 to 0.18 at 10^{-4} ampere (corresponding to final gains of 9.1 and 5 respectively for an assumed initial gain of 50). These gain changes, as well as those at low doses, are quite prominent at the moderately low collector current of 10^{-4} ampere.

At 10^{-2} ampere, the spread and magnitude of $1/h_{FE}$ degradation are reduced but still significant, especially at higher doses. The spreads in radiation-induced surface damage at low doses are from 0.003 to 0.008 (final gains of 43 and 36 for the assumed initial value of 50) and at high doses the spreads are from 0.012 to 0.018 (final gains of 31 and 26).

Similar gain change versus collector current characteristics can be observed for the Motorola 2N2222 in Figures 6-15 and 6-16 for small and large doses respectively, and for the Fairchild 2N2222 in Figures 6-17 and 6-18. The spreads in damage for the Motorola 2N2222 for the low and high doses respectively, are from 0.021 to 0.28, and from 0.042 to 0.16 at 10^{-4} ampere. At 10^{-2} ampere, the corresponding spreads are 0.002 to 0.011 and 0.004 to 0.018. For the Fairchild 2N2222, the spreads of $\Delta \frac{1}{h_{FE}}$ at 10^{-4} ampere are from 0.04 to 0.18 and 0.05 to 0.120, and at 10^{-2} ampere, from 0.003 to 0.007 and 0.005 to 0.012.

A tabulation of the minimum and maximum levels of gain degradation for all types of transistors evaluated is provided in Table 6-2. A matrix of data is presented for each device type consisting of the minimum and maximum gain degradation experienced by all transistors of a particular type, at two dose levels (small dose of $< 10^5$R and large dose ~ 10^7R) and at two collector current levels – one low compared to normal operation, the other near normal operating currents. To permit a comparison of devices on as nearly the same basis as possible, gain degradation data were normalized to the same relative value of collector current with respect to the normal operating current for that device. For example, to compare data taken at 10^{-4} ampere from a device that nominally operates at 10^{-1} ampere, the equivalent data from a device that nominally operates at 1 ampere would have to be taken at 10^{-3} ampere. The nominal operating current for each device for which comparisons were made in this report was assumed to be at the valley of the $\Delta \frac{1}{h_{FE}}$ vs I_C curve (corresponds to the peak of h_{FE} vs I_C curve). The two current levels chosen for comparing data were three decades and one decade below the nominal (minimum $\Delta \frac{1}{h_{FE}}$) value.

Table 6-2 - Spreads of $\Delta\frac{1}{h_{FE}}$ before screening

Transistor	Current Used For Evaluation (A)	Spread of $\Delta\frac{1}{h_{FE}}$ before screening (data x 10^{-3})			
		Small Dose		Large Dose	
		Min	Max	Min	Max
2N1613	10^{-4}	26	230	90	180
	10^{-2}	3	8	12	18
2N2222 (Mota)	10^{-4}	21	280	42	160
	10^{-2}	2	11	4	18
2N2222 (FSD)	10^{-4}	40	180	50	110
	10^{-2}	3.3	7	5	12
2N2905	10^{-3}	24	84	130	240
	10^{-1}	3.	7	1.6	1.8
2N1132	10^{-4}	18	540	95	440
	10^{-2}	2.6	27	10	27
2N722 (TI)	10^{-4}	40	76	157	240
	10^{-2}	6	8.5	13	18
2N722 (Mota)	10^{-4}	160	350	270	1000
	10^{-2}	16	28	30	55
2N3058	10^{-4}	40	100	65	160
	10^{-2}	15	30	20	47
2N3964	10^{-4}	50	135	560	760
	10^{-2}	4.2	11	31	40
2N2219A (metallized)	2×10^{-4}	54	65	90	100
	2×10^{-2}	5.1	6.3	11.8	13
2N2219A (nonmetallized)	2×10^{-4}	50	190	110	130
	2×10^{-2}	3.3	---	12.5	13.5
TD106 (metallized)	10^{-5}	21	40	140	160
	10^{-3}	3.3	6.2	18	20
TD106 (nonmetallized)	10^{-5}	6.8	920	180	1500
	10^{-3}	6.8	30	13.5	38

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6.2.2 Bipolar p-n-p Transistors

In contrast to n-p-n transistors, typical bipolar planar p-n-p transistors characteristically develop a channel component at small dose that increases in effectiveness as dose increases. This characteristic is demonstrated in Figures 6-35 and 6-36, which are typical plots of n versus ϕ for two p-n-p device types. These are typical of results in all the planar p-n-p types tested. The nonplanar Crystalonics 2N3058, on the other hand, had n values from 1.2 to 1.6 at both low and high doses. This device, which has an epitaxial collector with mesa structure emitter and base regions, reacts differently to ionizing radiation than does the SiO_2 passivated planar structure discussed in Section 6.2.3.

Changes in junction capacitances observed for the p-n-p transistors had no particular pattern. In some devices junction capacitances tended to increase slightly or remain constant at low radiation doses. Junction capacitances at large doses were observed to increase, decrease, or remain nearly constant so that no typical response was apparent.

Plots of $1/h_{FE}$ and I_{CBO} degradation with radiation are shown in Figures 6-4, 6-5, and 6-6, for three different types of p-n-p planar transistors (2N2905, 2N1132, and 2N722). The significant difference in radiation-induced degradation for n-p-n and p-n-p planar bipolar transistors is that channeling develops in both types at low doses and recedes for larger doses in n-p-n devices, but continues to build up with increases of dose in p-n-p devices. Hence p-n-p transistors appear to be more suitable for low dose applications (10^5R) while n-p-n transistors are preferred for higher dose applications. Such general conclusions cannot be drawn, however, since variations within a single type are often greater than the differences between n-p-n and p-n-p types.

Typical $\Delta \frac{1}{h_{FE}}$ vs I_C characteristics of the SiO_2 passivated planar p-n-p transistor for low and high doses respectively are presented in Figures 6-19 and 6-20 for the Motorola 2N2905, in Figures 6-21 and 6-22 for the Texas Instruments (TI) 2N1132, and in Figures 6-23 and 6-24 for the TI and Motorola 2N722. Values of $\Delta \frac{1}{h_{FE}}$ at two current levels (one three decades below the minimum and the other — one decade below) and two levels of radiation are given in Table 6-2.

The increase in the magnitude and the spread of damage for p-n-p devices at high dose levels compared to those at low doses or compared to n-p-n devices is evident from the table. The behavior of the TI 2N1132 was unusual in that after a large dose the worst transistor of the group improved over its small dose value. However, the TI 2N722, which is the same as the 2N1132 except for packaging, behaved as expected for a p-n-p device. Diferences between the TI 2N722 and Motorola 2N722 are significant as evidenced by the table and the curves of Figures 6-23

and 6-24. It is not clear whether this distinction can be construed as an improved processing technique for that device or whether it is simply indicative of the particular sampling used for the tests. It is certain, however, that general comparisons cannot be made among manufacturers because often the same manufacturer will have the best of one type of device and the worst of another.

6.2.3 Nonplanar Transistors

Three nonplanar bipolar transistors were evaluated. One, the Crystalonics 2N3058 was a low-level switch having an epitaxial collector with mesa structure emitter and base regions. The other two were power transistors; one was the Silicon Transistor Corporation STC 1739 single diffused mesa transistor, and the other type was a Westinghouse 2N2771 alloy junction transistor.

The characteristic behavior in ionizing radiation of nonplanar devices without SiO_2 passivation was aptly described by Peck,[5.1] Estrup[6.1] and others. The purpose for including them in this program was to compare their behavior with planar SiO_2 passivated devices under the same test conditions, and to obtain specific results on the two power devices which NASA-MSFC is considering for applications that may involve ionizing radiation.

As noted by Peck,[5.1] the response of non SiO_2 passivated transistors was heavily dependent on bias and radiation rate as well as the total dose. The model proposed was that h_{FE} and I_{CBO} degradations were due to surface channels produced by an accumulation of charged ambient gas ions on the device surface. The gas ions are attracted to the transistor surfaces by electric fields produced when the device is electrically biased. Hence when the bias is removed (such as for taking gain measurements), the damage decays back to zero. Or if the radiation is removed, the damage again decays back to zero but with a different (longer) time constant.

This rapid recovery of damage with bias or radiation removal by nonplanar transistors is in sharp contrast to the long, essentially permanent storage of damage in planar SiO_2 passivated devices. Consequently, the techniques used for measuring damage to planar transistors (radiation removed and wide range of forward biases applied) are not applicable to nonplanar transistors. This was particularly evident with the two power transistors tested. The results of taking measurements in the usual way are shown in Figures 6-7 and 6-8 for the STC1739 and the 2N2771 respectively. Damage annealing between the time the radiation source was turned off and the measurements were taken is thought to be the reason why very little damage was observed. Peck and other early experimenters reported this same effect.

To circumvent this rapid recovery during measurements, measurements were made during radiation and with the bias left unchanged. This meant that only leakage current measurements could be made, not gain

which required forward biasing at different levels. Rather than attempt to measure gain on the nonplanar power transistors, the two transistors were operated in the same manner as in their intended application, and the output was examined for degradation while the transistors were being irradiated. Half the power transistors of each type were tested in this manner, and the other half were reverse-biased for leakage current measurements during irradiation.

The operating mode was achieved by driving the transistors with a 400Hz square wave on the bases with I_C = 4.5A and I_B = 400mA during saturation and V_{CE} = 56V during cutoff. With the base drive used, good square wave responses were obtained at the collectors. Differences in data as a result of the different biases used (switching and reverse bias) were undetectable.

The switched transistors were irradiated to 2 x 10^6 rads without any observable changes in the square wave output. The conclusion, therefore, is that both power transistors are suitable for ionizing radiation environments provided they are continuously switched on with at least a 50 percent duty cycle.

The same devices left in the off or reverse biased condition would not be suitable for radiation environments since their leakage currents would be excessive after modest radiation doses (in the milliampere range after 10^5 rads) and could turn normally off devices on.

The response of nonplanar devices to ionizing radiation is clearly not as predictable nor as repeatable as that of planar devices. The amount of damage incurred in nonplanar transistors is heavily dependent on bias and radiation dose rate.

The ionizing radiation characteristics of the Crystalonics 2N3058 were found to be a combination of planar and mesa characteristics as expected because of its construction. Gain variations with radiation were comparable to those experienced by other planar devices since the 2N3058 does have a planar emitter-base junction. Leakage current changes, however, were similar to those observed in mesa devices because the 2N3058 has a mesa collector-base junction.

Gain and leakage current variations with radiation are shown in Figure 6-9. Gain changes are moderate but the spread is relatively small and they are repeatable, the second cycle indicating that gain did recover. In contrast, leakage current changes were quite large and were not repeatable. Since the device is basically a low level switching device, large changes in leakage current can be catastrophic for many applications.

The changes in gain of the 2N3058 as a function of current at a low and a high dose level are shown in Figure 6-25 and 6-26 respectively. The variations in magnitude and spread are shown in Table 6-2 for two different current levels. They appear to be typical of the more stable types of p-n-p devices.

6.2.4 Evaluation of Special Processes

6.2.4.1 Processes Evaluated

One of the primary purposes of the Phase II experiments was to evaluate transistors manufactured with special processes designed specifically to improve surface stability. Three of the processes evaluated – Fairchild's Planar II, Texas Instruments' Tri Rel (field plate), and Motorola's annular (guard ring), are used on commercially available devices. Other transistors included in the evaluation to determine the effects of metallization over the emitter-base junction are specially modified experimental n-p-n transistors supplied by Motorola (2N2219A) and Fairchild (TD106). The effects of metallization are readily evaluated from these devices because samples of the same devices with and without metallization were supplied.

A discussion of the results obtained from the experiments is presented in this section; however, it should be noted that these experiments were performed on small sample sizes and that final conclusions as to the relative merits of these processes should not be based on these results.

6.2.4.2 Planar II Process, Fairchild

The Planar II process is an outgrowth of MOSFET technology wherein attempts were made to develop stable devices by developing a high quality alkali-free oxide. The Fairchild 2N3964 p-n-p transistor was used to evaluate this process.

Six 2N3964 transistors were irradiated to doses approaching 10^7 rads. Data on $1/h_{FE}$ and I_{CBO} taken at a low dose level and at the end of the test are shown graphically in Figure 6-10. In addition, curves of $\Delta \frac{1}{h_{FE}}$ as a function of collector current are shown in Figures 6-27 and 6-28 for low and high doses respectively. The data indicate that this transistor is comparable in sensitivity to ionizing radiation to the more vulnerable p-n-p devices tested in this program as shown in Table 6-2. I_{CBO} buildup is a more gradual function of dose; but after about 10^7R, it is about the same as the Texas Instruments or Motorola 2N722. The slope constants n indicate that at low doses the devices develop channel components that increase very little with increases of dose to about 10^7R. The n values are also very closely grouped and nearly repeatable, implying that the surface properties of all of the transistors tested are about the same and that the oxide interface is of high quality.

6.2.4.3 Tri Rel (Field Plate), Texas Instruments

Tri Rel is a three-stage process to improve the reliability of small signal p-n-p devices. The process includes a metal

field relief electrode over the oxide of the collector region, a highly p-doped guard ring diffused into the collector region, and an oxide thermal stabilization technique in which a phosphorus glaze is left over the surface of the oxide to act as a getter for sodium and potassium ions. The 2N722 and 2N1132 were used to evaluate Tri Rel.

Results of irradiation tests on these transistors are discussed in Section 6.2.2 on p-n-p transistors. $1/h_{FE}$ and I_{CBO} damage buildup characteristics with radiation are given in Figures 6-5 and 6-6. Variations in $\Delta \frac{1}{h_{FE}}$ with current for small and large doses are given in Figures 6-21 through 6-24. Several TI 2N1132 devices had large h_{FE} degradation at low doses, which casts doubt on their effectiveness as radiation-tolerant devices without screening. Also, the spreads of h_{FE} damage characteristics for the 2N1132 were much wider for the second cycle, with some devices improved and others worse, indicating random changes in surface properties. On the other hand, the TI 2N722 showed very little damage, and the damage observed was very repeatable in the second cycle. Since both devices are made from chips by the same process except for packaging (the 2N1132 as a TO5 and the 2N722 as a TO18), differences in response can only be attributed to the small sample sizes and different batch characteristics.

Channels developed in the 2N1132 at low doses as shown by the slope constants of Figure 6-36 and became worse with increases in dose, indicating that the surface channeling problem in ionizing radiation is not eliminated by the Tri Rel process.

6.2.4.4 Annular Process, Motorola

The Motorola annular process uses a highly p-doped annular ring in the collector region on both n-p-n and p-n-p devices. The 2N2222 n-p-n and the 2N2905 p-n-p transistors are examples of this process that were used for evaluation. Damage response characteristics were shown previously in Figures 6-2 and 6-4 respectively and damage variation with current in Figures 6-15, 6-16, 6-19 and 6-20.

The 2N2222 n-p-n device is relatively unaffected by the guard ring as expected since the major collector channeling problem is with inversion of the low-doped p-collector of p-n-p devices. Also, the h_{FE} and I_{CBO} degradation for the 2N2905 devices was not significantly different from that of other p-n-p's. Channel components at low doses were detected by n values as shown in Figure 6-34 for the 2N2222 and 6-35 for the 2N2905. The channels receded in the n-p-n device but continued to increase in the p-n-p device, indicating that the annular process does not eliminate the channeling problem induced by ionizing radiation.

6.2.4.5 Specially Modified 2N2219A, Motorola

Six Motorola 2N2219A n-p-n transistors were modified by Motorola with metallization over the emitter-base junction. These six were irradiated along with six normal 2N2219A transistors to ascertain the effectiveness of emitter-base metallization for reducing base-emitter channels. The results are shown in Figure 6-11, where devices 1 through 6 are those with metallization.

Note that the devices with metallization have less h_{FE} damage buildup and are more tightly grouped than the nonmetallized devices. The metallized group also recovered better and repeated damage buildup better than its nonmetallized counterpart. The conclusion from these results is that emitter-base channeling is effectively inhibited by the metallization. This conclusion is also supported by the n values at small doses in Figure 6-37. Damage buildup characteristics for I_{CBO} are unaffected by the metallization, as expected since I_{CBO} is a collector base junction property.

Spreads of $\Delta \frac{1}{h_{FE}}$ vs I_C characteristics for the 2N2219A at small and large doses are presented in Figures 6-29 and 6-30. After a small dose, the $\Delta \frac{1}{h_{FE}}$ spread three decades below the minimum (2×10^{-4}A) for those transistors with metallization over the emitter-base junction is 0.055 to 0.065 and for the nonmetallized group, 0.05 to 0.19. After a large dose, the damage spread for the metallized transistors is 0.09 to 0.1 and 0.11 to 0.13 for the nonmetallized devices. Damage spreads for the metallized transistors are smaller and these devices accrue less h_{FE} degradation than their nonmetallized counterparts, particularly at low currents where channel currents dominate at low doses. This is also true at large doses after the dominant channel mechanism is known to have diminished.

The conclusion regarding metallization over the emitter-base junction is that it is very effective in minimizing the magnitude and spread of damage at low currents and low doses. For high currents or high doses, metallization has less effect.

6.2.4.6 Experimental TD106, Fairchild

Twelve TD106 n-p-n devices were made available by Fairchild; six of these were fabricated with a metal gate over the emitter-base junction. Three cycles of bias-radiation and recovery stresses were used to evaluate the devices in radiation. The second cycle was a repetition of the first, in which three of the metallized devices were biased with a gate-base bias of -6V and three with a gate-base bias of -24V. In the third cycle, no gate bias was used. Some of the metallized devices were destroyed because of their extreme sensitivity to induced electrostatic charge.

Results of irradiation tests are shown in Figure 6-12 where it can be observed that the metallized group sustained less h_{FE} degradation. n values for the metallized group indicate that emitter-base channeling was prevented but that gate biasing played no discernible role during irradiation. This also can be observed in Figure 6-12. Gate-base bias during measurement was relatively ineffective because not enough bias could be applied to the gate to mask the damage. n values also indicate that for those transistors without metallization the channel component increased rather than decreased after a dose of $\phi > 10^7$R, similar to the response of p-n-p rather than n-p-n devices. This may be the result of a relatively low carrier concentration in the base region[6.2] facilitating inversion of the p-material and restraining the electron emission mechanism.

Spreads of $\Delta \frac{1}{h_{FE}}$ vs I_C characteristics for the TD106 are shown in Figures 6-31 and 6-32 for small and large doses. The spread of $\Delta \frac{1}{h_{FE}}$ for those transistors with metallization over the emitter-base junction varies from 0.022 to 0.04 at 10^{-5}A (three decades below the minimum) after a small dose. After a large dose, the spread for these devices is 0.14 to 0.16 at 10^{-5}A. For the nonmetallized transistors, the low dose spread at 10^{-5}A extends from 0.07 to 0.92 and after a large dose the spread becomes 0.18 to 1.5. The metallized transistors group tighter and do not degrade as much as the nonmetallized transistors at low currents. These data again substantiate the effectiveness of emitter-base metallization for minimizing the magnitude and spread of gain degradation at low currents.

6.2.5 MOSFET

Phase II investigations included a test of 12 p-channel, enhancement mode metal-oxide-semiconductor field effect transistors (MOSFET), the General Micro-electronics Incorporated (Philco Corporation) 2N3609. Special instrumentation consisting of a logarithmic amplifier and analog plotter to automatically plot many decades of data was used to record the drain-source current I_{DS} as a function of gate voltage V_G to determine the effects of bias and ionizing radiation on these devices. The devices tested had two transistors built on a single monolithic chip since these devices are intended for use in differential amplifier applications. For this investigation, one transistor on each chip was biased on with a gate voltage of -5V, while the other was biased off with +5V to demonstrate the effects of bias during radiation. Since the devices are initially well matched, this bias during irradiation was chosen as a worst case condition for producing mismatch.

Figure 6-40 shows typical I_{DS} vs V_G characteristics at various doses for both on and off biased transistors of a chip. The numbered curves represent those transistors which were biased on during radiation; the lettered curves represent those biased off during radiation.

The minus gate voltage on the gate causes enhancement of a p-channel in the semiconductor beneath the gate, which turns the transistor on. Ionizing radiation causes a positive charge buildup to occur in the silicon dioxide, and hence the negative voltage V_G required to turn on the transistor increases with dose; but the negative bias on the gate during irradiation has an attenuating effect on this positive charge buildup. The numbered sequence of characteristics in Figure 6-40 shows the change of transconductance characteristic of the negatively biased 2N3609 transistors as a function of dose. Changes in transconductance are small with radiation, but the operating current range is reduced due to increased leakage current.

The typical bias dependent drain source leakage current I_{DSX} that exists when the transistor is shut off increases from about 0.1nA (curve 1) to about 20μA (curve 4) as a function of dose for $\phi \leq 5 \times 10^5$R and then decreases for increases in ϕ similar to channel buildup and recession in SiO_2 passivated n-p-n transistors. It is interesting to observe that I_{DSX} as a function of ϕ is independent of V_G (shown by vertical portion of curves) until $\phi > 5 \times 10^5$R, at which time it has voltage dependency that changes with ϕ. I_{DSX} is an increasing function of increasing negative V_G prior to the turn-on threshold voltage of V_{GTH}.

In addition to the increase in leakage current, the turn on voltage increases about a factor of 2 as shown by the curves. Positive gate voltage biases the transistor so that the p-type silicon beneath the gate is depleted of positive charge carriers and the transistor is biased off. Ionizing radiation again causes the silicon dioxide at the silicon-oxide interface to become positively charged, and this effect is further enhanced by the bias. Hence a larger negative bias is required to turn on the transistor that was biased off during irradiation than the one biased toward enhancement (on) during irradiation. Figure 6-40 shows from the lettered sequence of characteristics, that typically the transistors will not turn on even for the maximum allowable gate voltage for $2.5 \times 10^4\text{R} \leq \phi \leq 6 \times 10^6$R. For $5 \times 10^5\text{R} < \phi < 10^7$R, those transistors that would not turn on at lower radiation doses begin to recover. At $\phi \doteq 10^7$R, the transconductance portion of the characteristics are similar to those for the transistors biased on during irradiation, but the turn on voltage is much greater.

I_{DSX}, which was independent of V_G prior to irradiation, becomes a decreasing function of negatively increasing V_G as early as 10^4R for MOSFETs biased positively during irradiation.

The high temperature recovery stress (320°C for a period of five hours) did not fully return the devices to their initial conditions. The transconductances of both transistors on each chip were initially very well matched, as can be seen from Figure 6-40. After recovery, the difference in V_G over most of the transconductance curves is about 1.5V. In some cases, I_{DSX} did not recover to initial conditions. The effects of reirradiation are similar to first cycle damage responses.

A single n-channel MOSFET, Motorola MM2102, was also irradiated to study the behavior of channel recession at large doses. If channel recession results from the transfer of electrons into the oxide, the n-channel MOSFET with a positive gate bias should behave in radiation similar to the p-type base region of an n-p-n transistor with a reverse-biased collector base junction during irradiation. Behavior was as predicted, with a channel forming rapidly at low doses, followed by a gradual recession of the channel at large doses.

The MM2102 was irradiated at a rate of 5×10^5R/hr with the drain and source leads at ground and +6V potential on the gate lead. The drain to source resistance R_{DSS} with V_{GS} = 0V was measured at intervals during irradiation. Before irradiation, R_{DS} was greater than 1 megohm, indicating that no substrate channel was present. By 8×10^3R (the first measurement) a channel had formed, reducing R_{DSS} to 26 ohms. A gate bias of +20V during measurement increased R_{DS} to 34 ohms. Figure 6-41 shows how channel conductance $1/R_{DSS}$ varied with X-ray exposure. Maximum channel conductance is reached at about 10^5R followed by a gradual decrease. By 3×10^7R (the last measurement) the conductance is down to 20 percent of its peak value and appears to be still decreasing. It is interesting to compare the shape of this curve with that of Figure 4-9 of Section 4-4 for a bipolar n-p-n transistor. Both figures have similar early shapes and peak at approximately the same dose.

The results of these and other experiments[6.3] indicate that the sensitivity of MOS devices to radiation damage is a function of the magnitude and polarity of the gate bias during irradiation. Because of an apparent buildup of positive charge in the SiO_2, it has been determined from these and other experiments[6.4, 6.5] that for low amounts of radiation and no positive bias, carefully selected enhancement devices can be used in ionizing radiation. Transconductance changes are relatively small but leakage current changes are large and turn-on voltage increases. Devices biased positively during irradiation are rendered almost useless even by small radiation doses. The p-channel, enhancement mode MOSFET is apparently the more tolerant of the MOS devices.[6.4]

6.2.6 Junction FET

A set of 12 Siliconix 2N3387 p-channel junction field effect transistors (JFET) were evaluated. These devices are encapsulated in ribbon lead ceramic disc "FlatPacs." The transistors are depletion mode devices, i.e., they normally conduct until biased positively enough to cause the junction depletion regions to spread into the channel region, thereby turning the transistor off.

During irradiation, the transistors were biased with V_{GS} = + 10V and the drain and source terminals shorted to ground. The bias was more than sufficient to cause the transistors to be off. The dose rate used was 5×10^5R/hr. Figure 6-42 shows two cycles of typical I_{DS} vs V_G characteristics as a function of dose. The numbered sequence of characteristics pertains to the first cycle; the lettered sequence, to the second cycle.

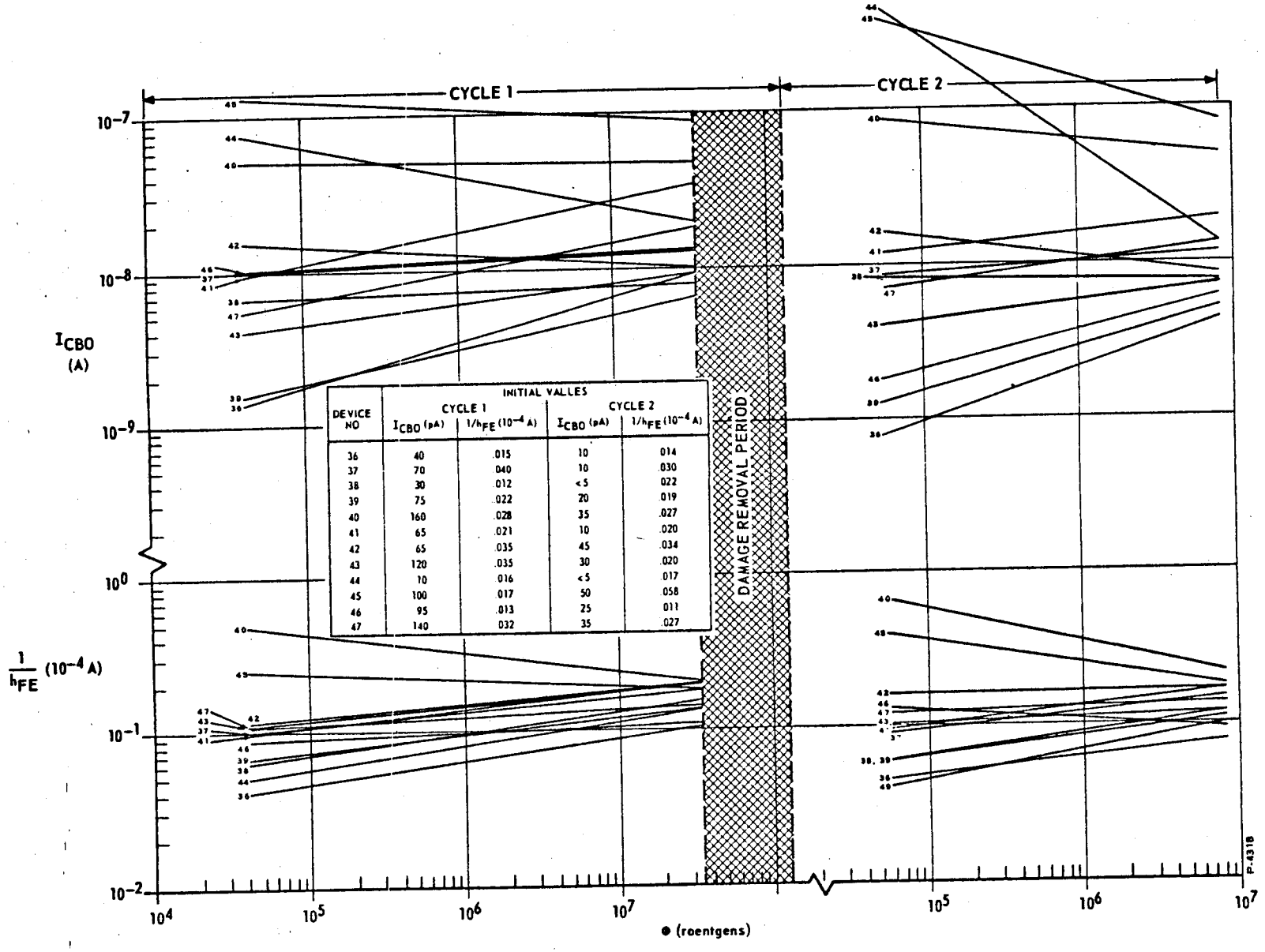
The characteristics indicate that the transconductance is almost unaffected by ionizing radiation to $\phi = 10^7$R. Prior to radiation, I_{DS} is in the nanoampere range, with V_{GTH} near 6V. Typically, I_{DSX} increases to near 10^{-8}A at $\phi \doteq 1.5 \times 10^6$R and then decreases with increased dose. The effects appear to be similar to I_{CBO} changes seen for bipolar n-p-n devices where channels are observed to increase with dose until a discharging mechanism occurs to cause the channel to recede.

Recovery was observed to be excellent using the 320°C temperature stress for a period of five hours. When the transconductance curves of the second cycle were super imposed upon those of the first, they indicated excellent repeatability. Leakage currents were not as large on the second cycle as the first, indicating that surface properties were somewhat improved as a result of the screening test.

Results of the experiments on FETs showed that junction FETs are virtually unaffected by ionizing radiation to levels of 10^7R.

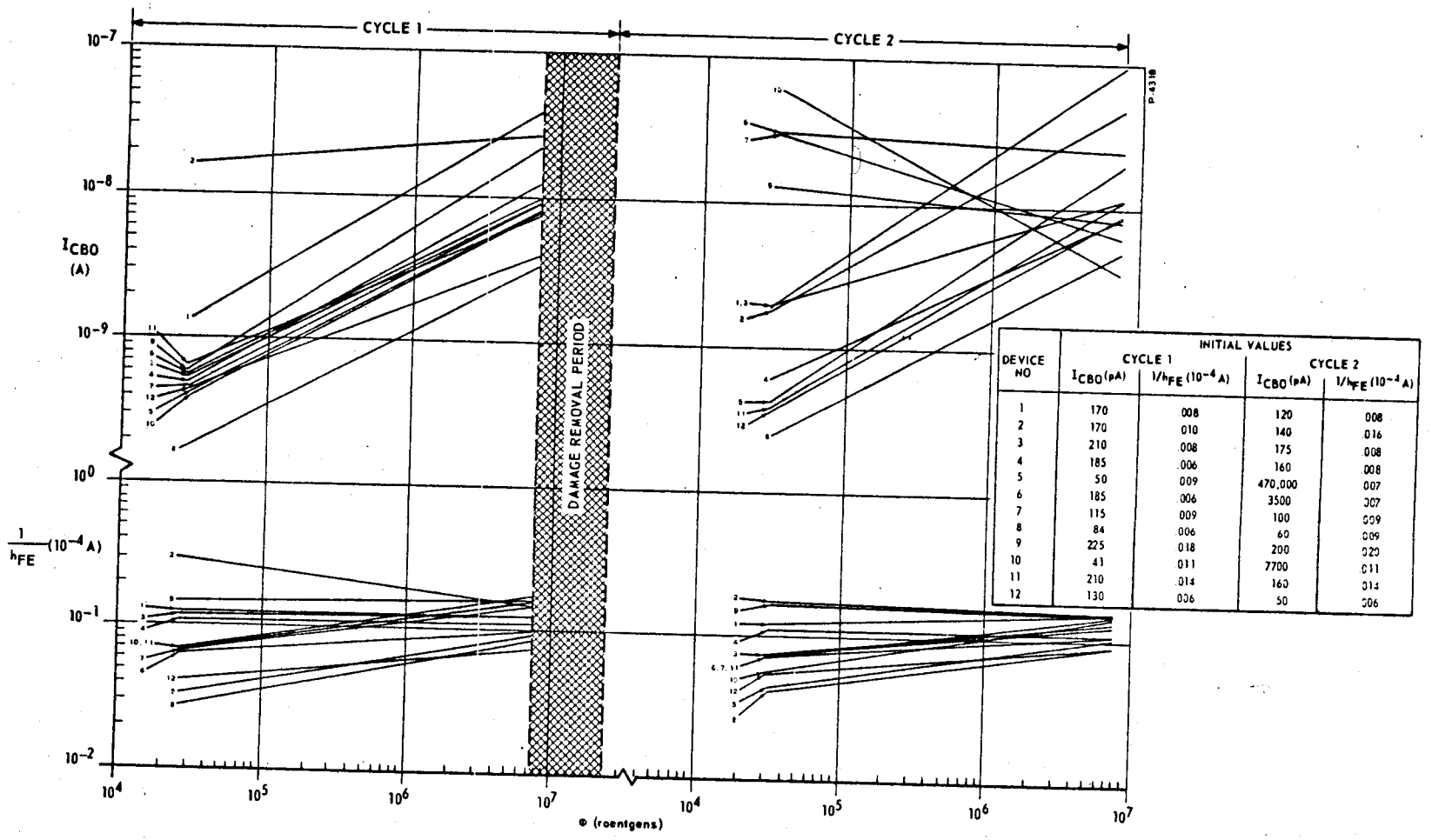
6.3 MODEL REFINEMENTS FROM PHASE II EXPERIMENTAL RESULTS

A modification of the model is proposed for p-n-p transistors with reverse biased collector-base junctions during irradiation. The aforementioned studies of the effects of ionizing radiation on MOS devices have also shown that either a positive or negative gate bias during radiation produces a positive charge buildup in the oxide layer. Grove and Snow[5.4] explain the behavior produced by a positive gate bias as a drift of electrons from generated electron-hole pairs away from the SiO_2 -Si interface, leaving trapped holes behind. The negative gate bias causes the electrons to drift to the SiO_2 -Si interface and cross this interface into the silicon, leaving the trapped holes behing in the oxide layer. Irradiation of a p-n-p transistor with a reverse-biased collector-base junction should produce charge buildup effects at the emitter-base junction similar to those for an MOS device with a negative gate. Thus the oxide surface is negatively charged by the ionized ambient gas, causing an ultimate positive charge buildup in the oxide. Since the positive charge is physically closer to the silicon than the oxide surface charge, the result is enhancement of the n-type base region and the depletion or inversion of the p-type emitter region. This causes a channel to grow by extending the junction into the emitter region instead of the base region as for n-p-n transistors. The fact that the channel did not recede at large doses with this model is not surprising since positive charge buildup is near the oxide surface rather than at the SiO_2 -Si interface. Electrons from the electron-hole pairs in the oxide were rapidly swept to the SiO_2 -Si interface by the oxide field and across the interface by emissions.



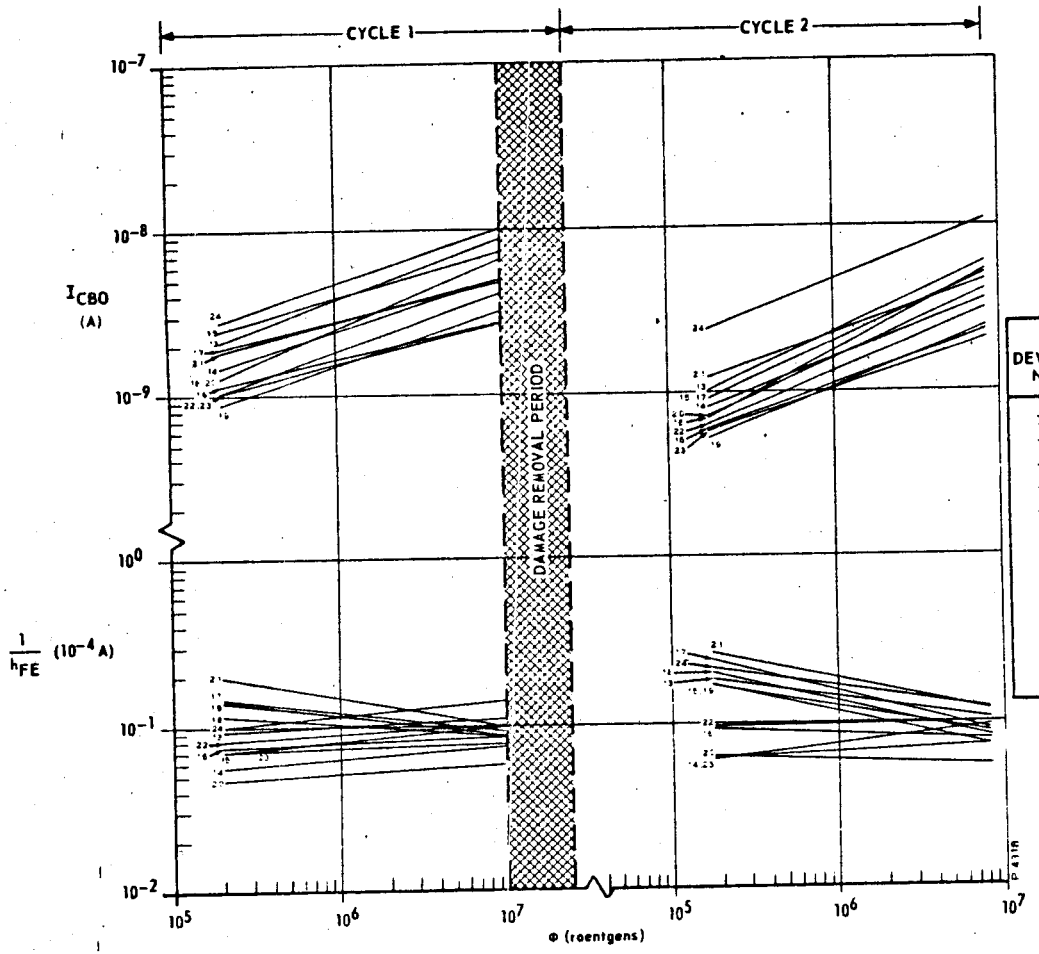
DEVICE NO	INITIAL VALUES CYCLE 1 I_{CBO} (pA)	CYCLE 1 $1/h_{FE}$ (10^{-4} A)	CYCLE 2 I_{CBO} (pA)	CYCLE 2 $1/h_{FE}$ (10^{-4} A)
36	40	.015	10	014
37	70	040	10	.030
38	30	.012	<5	022
39	75	.022	20	019
40	160	.028	35	.027
41	65	.021	10	.020
42	65	.035	45	.034
43	120	.035	30	.020
44	10	.016	<5	.017
45	100	.017	50	.058
46	95	.013	25	011
47	140	.032	35	.027

Figure 6-1 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, Fairchild 2N1613 (n-p-n)



DEVICE NO	INITIAL VALUES CYCLE 1 I_{CBO} (pA)	CYCLE 1 $1/h_{FE}$ (10^{-4} A)	CYCLE 2 I_{CBO} (pA)	CYCLE 2 $1/h_{FE}$ (10^{-4} A)
1	170	008	120	008
2	170	010	140	016
3	210	008	175	008
4	185	006	160	008
5	50	009	470,000	007
6	185	006	3500	007
7	115	009	100	009
8	84	006	60	009
9	225	018	200	020
10	41	011	7700	011
11	210	014	160	014
12	130	006	50	006

Figure 6-2 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, Motorola 2N2222 (n-p-n)



DEVICE NO.	INITIAL VALUES CYCLE 1 I_{CBO} (pA)	CYCLE 1 $1/h_{FE}$ (10^{-4} A)	CYCLE 2 I_{CBO} (pA)	CYCLE 2 $1/h_{FE}$ (10^{-4} A)
13	42	.023	<5	.021
14	40	.010	8	.009
15	40	.015	10	.018
16	30	.027	10	.019
17	15	.027	8	.023
18	20	.008	10	.009
19	50	.020	15	.015
20	45	.007	15	.007
21	35	.025	8	.024
22	28	.020	<5	.019
23	37	.016	<5	.014
24	62	.020	<5	.028

Figure 6-3 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, Fairchild 2N2222 (n-p-n)

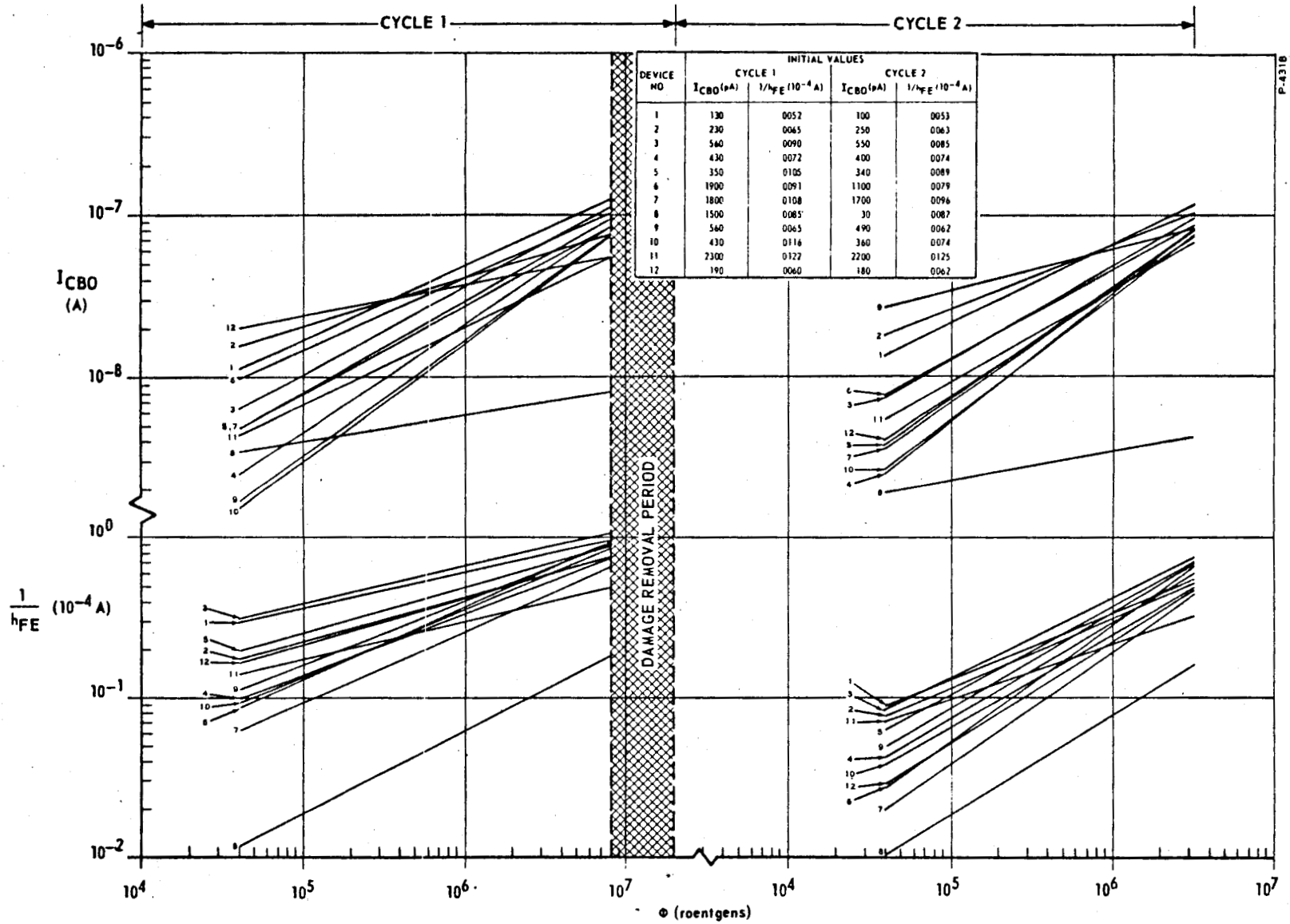
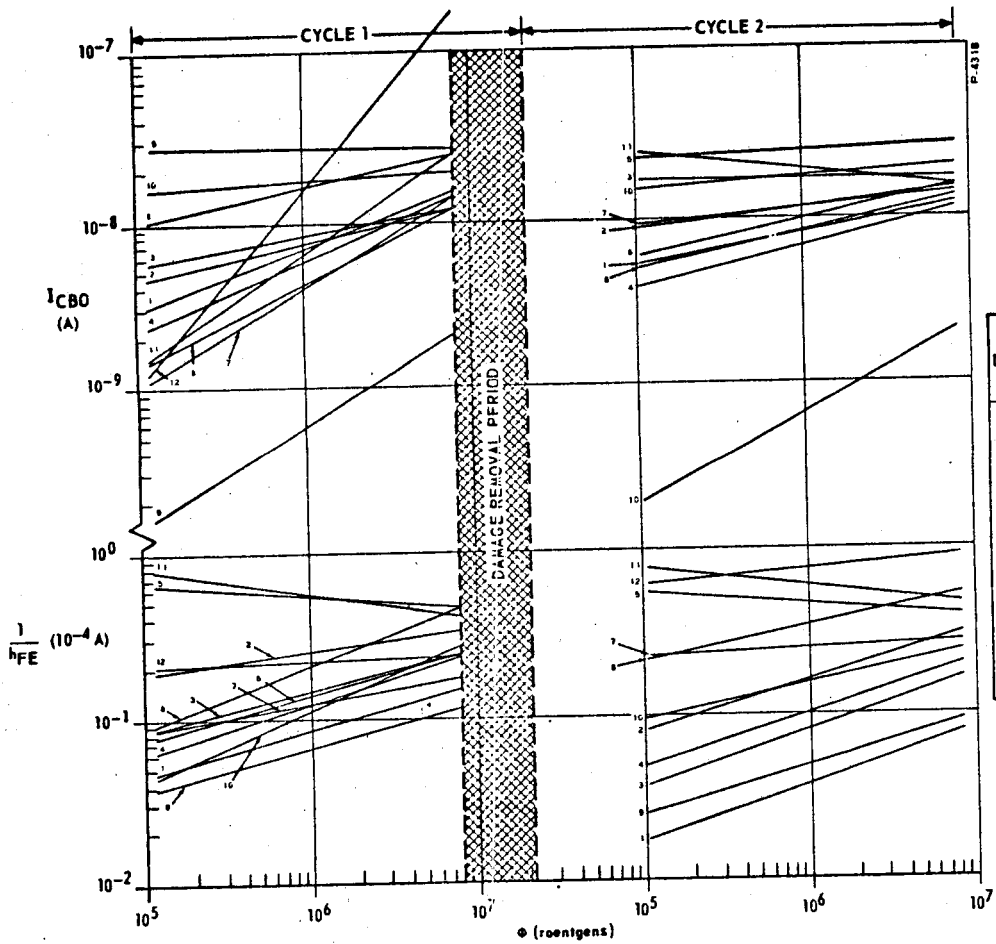
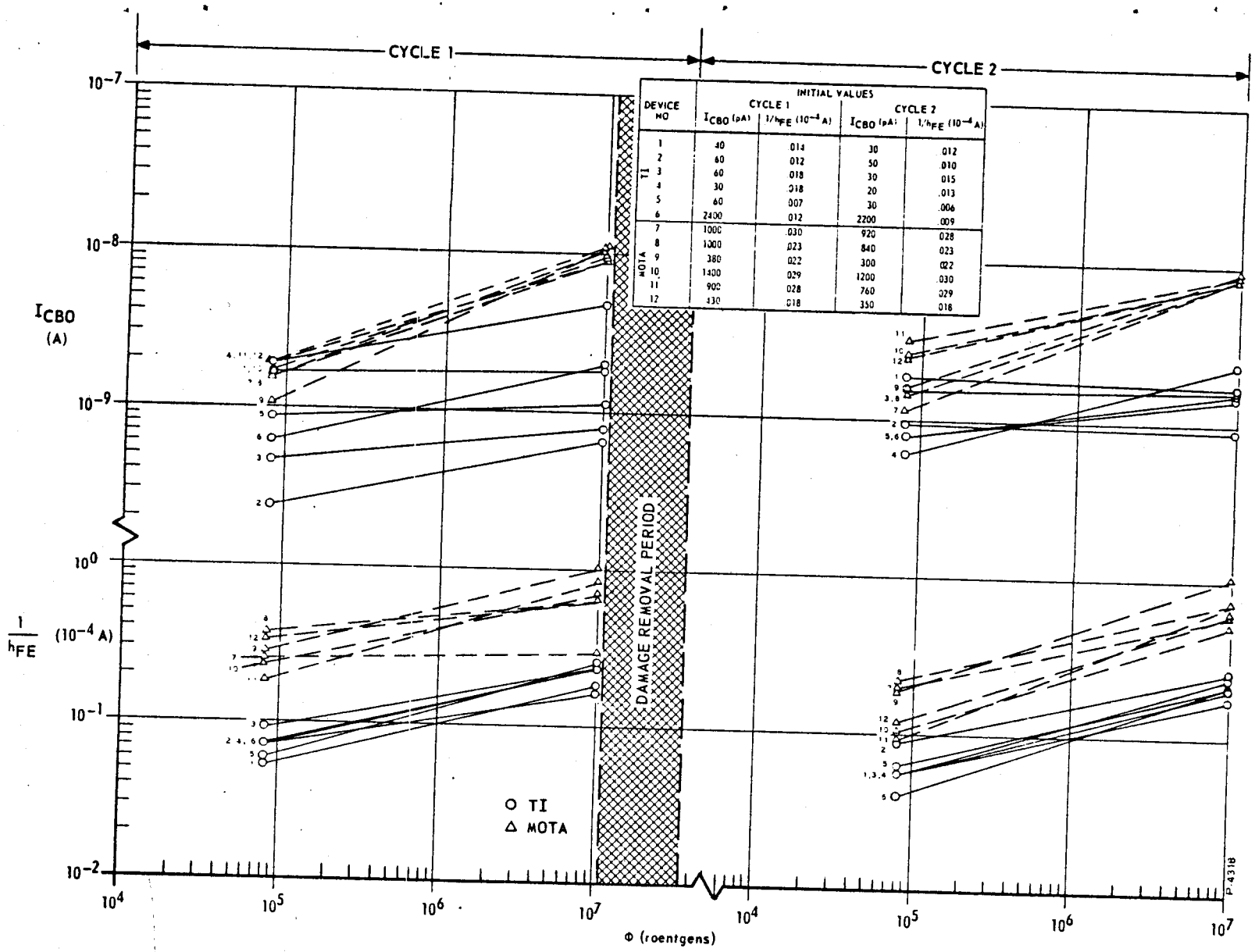


Figure 6-4 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, Motorola 2N2905 (p-n-p)



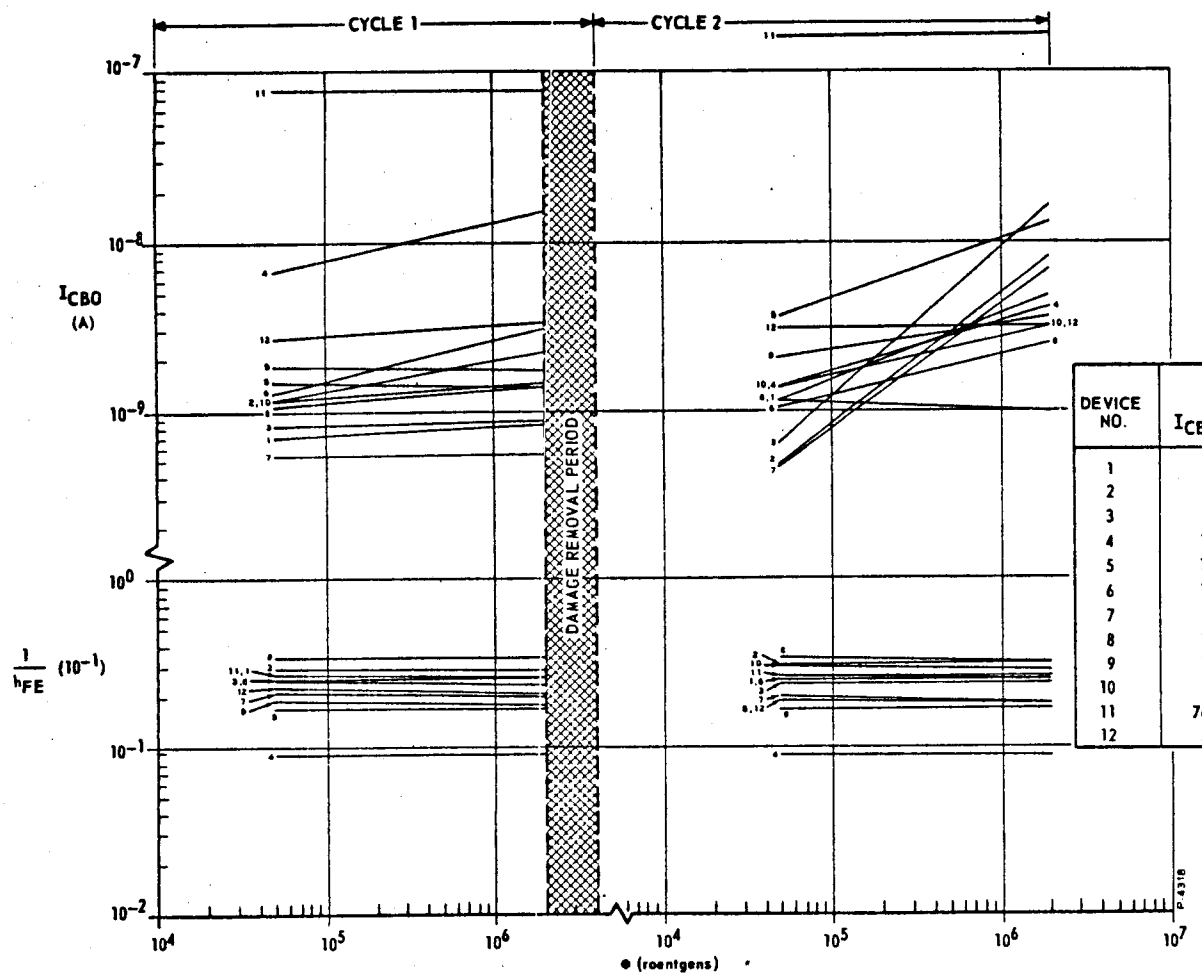
DEVICE NO.	INITIAL VALUES CYCLE 1 I_{CBO}(pA)	CYCLE 1 $1/h_{FE}$(10^{-4} A)	CYCLE 2 I_{CBO}(pA)	CYCLE 2 $1/h_{FE}$(10^{-4} A)
1	45	.013	20	.009
2	45	.043	20	.021
3	110	.021	20	.017
4	40	.017	20	.014
5	590	.208	370	.114
6	60	.026	420	
7	100	.023	65	.049
8	80	.031	30	.033
9	40	.021	20	.017
10	480	.017	240	.016
11	25	.192	20	.241
12	45	.152	865000	.579

Figure 6-5 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, Texas Instruments 2N1132 (p-n-p)



DEVICE NO		CYCLE 1 I_{CBO} (pA)	CYCLE 1 $1/h_{FE}$ (10^{-4} A)	CYCLE 2 I_{CBO} (pA)	CYCLE 2 $1/h_{FE}$ (10^{-4} A)
1	TI	40	.014	30	.012
2	TI	60	.012	50	.010
3	TI	60	.018	30	.015
4	TI	30	.018	20	.013
5	TI	60	.007	30	.006
6	TI	2400	.012	2200	.009
7	MOTA	1000	.030	920	.028
8	MOTA	1000	.023	840	.023
9	MOTA	380	.022	300	.022
10	MOTA	1400	.029	1200	.030
11	MOTA	900	.028	760	.029
12	MOTA	430	.018	350	.016

Figure 6-6 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, 2N722, Texas Instruments 1-6, Motorola 7-12 (p-n-p)



DEVICE NO.	INITIAL VALUES			
	CYCLE 1		CYCLE 2	
	I_{CBO} (nA)	$1/h_{FE}$ $(10^{-1}$ A)	I_{CBO} (nA)	$1/h_{FE}$ $(10^{-1}$ A)
1	80	.027	81	.026
2	45	.030	43	.031
3	29	.027	51	.025
4	127	.009	–	.009
5	144	.021	370	.019
6	119	.025	105	.025
7	55	.021	44	.020
8	112	.035	108	.034
9	166	.020	182	.017
10	112	.031	130	.030
11	7600	.028	18000	.026
12	255	.024	217	.020

Figure 6-7 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, Silicon Transistor Corporation STC1739 (n-p-n)

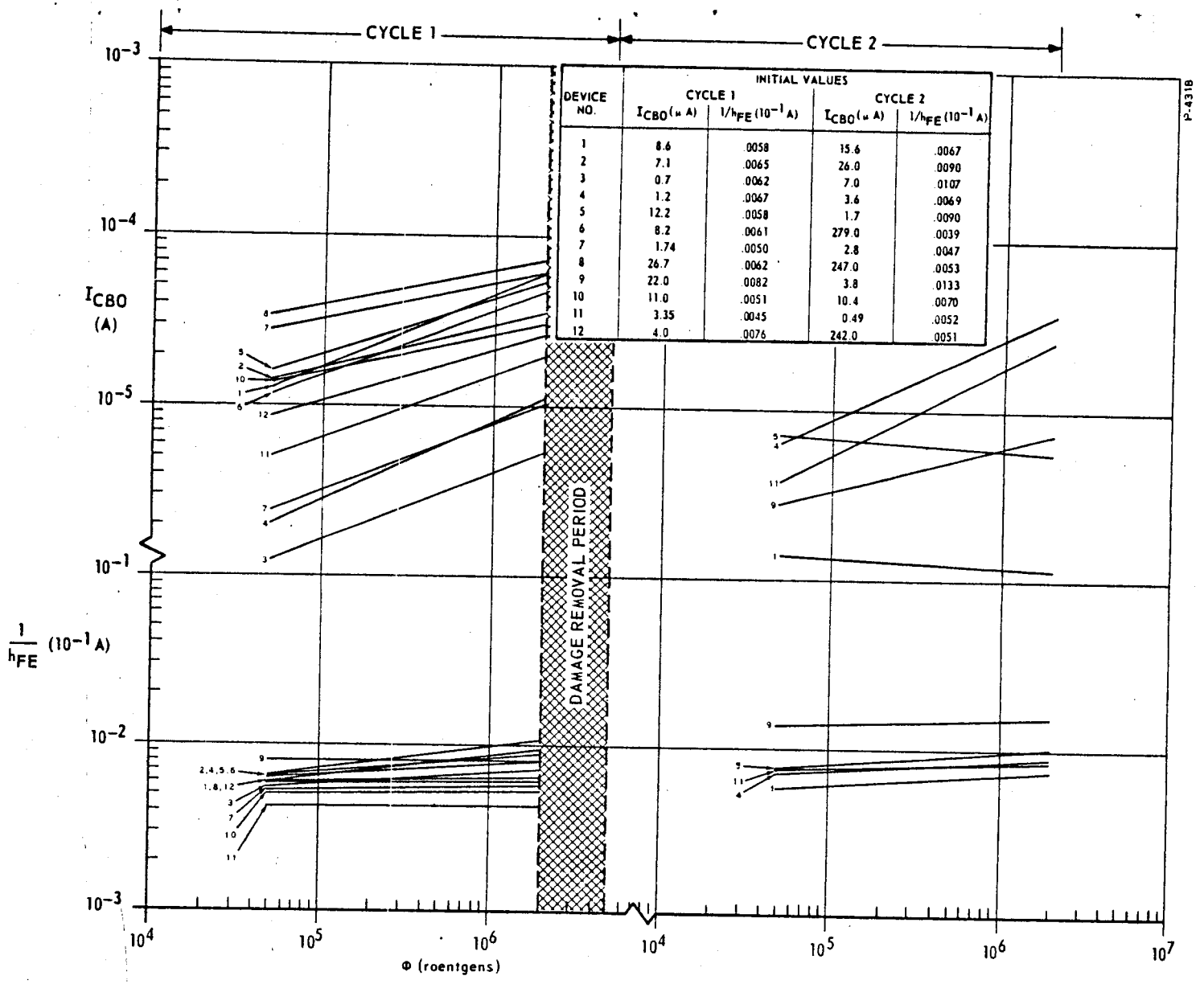
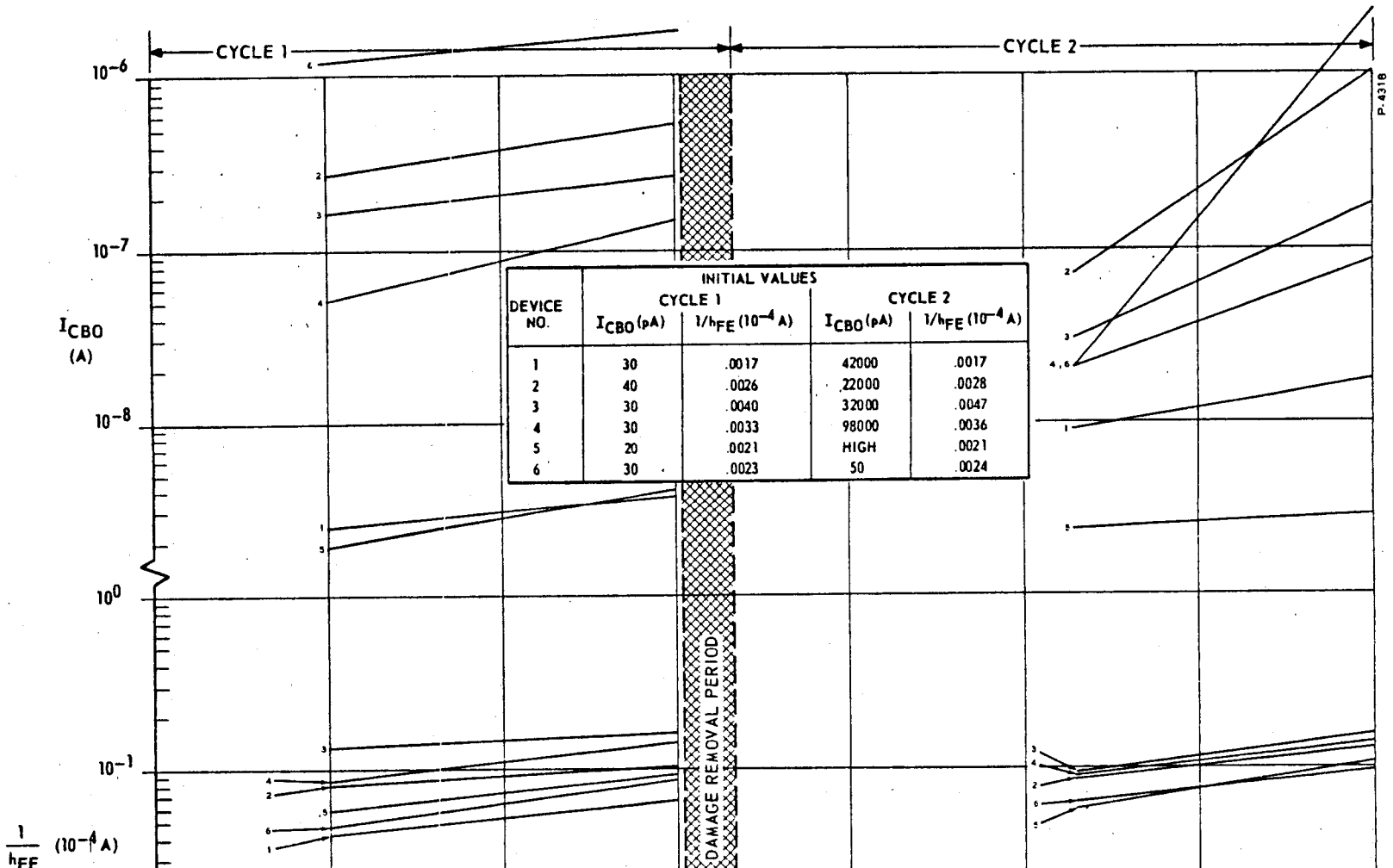
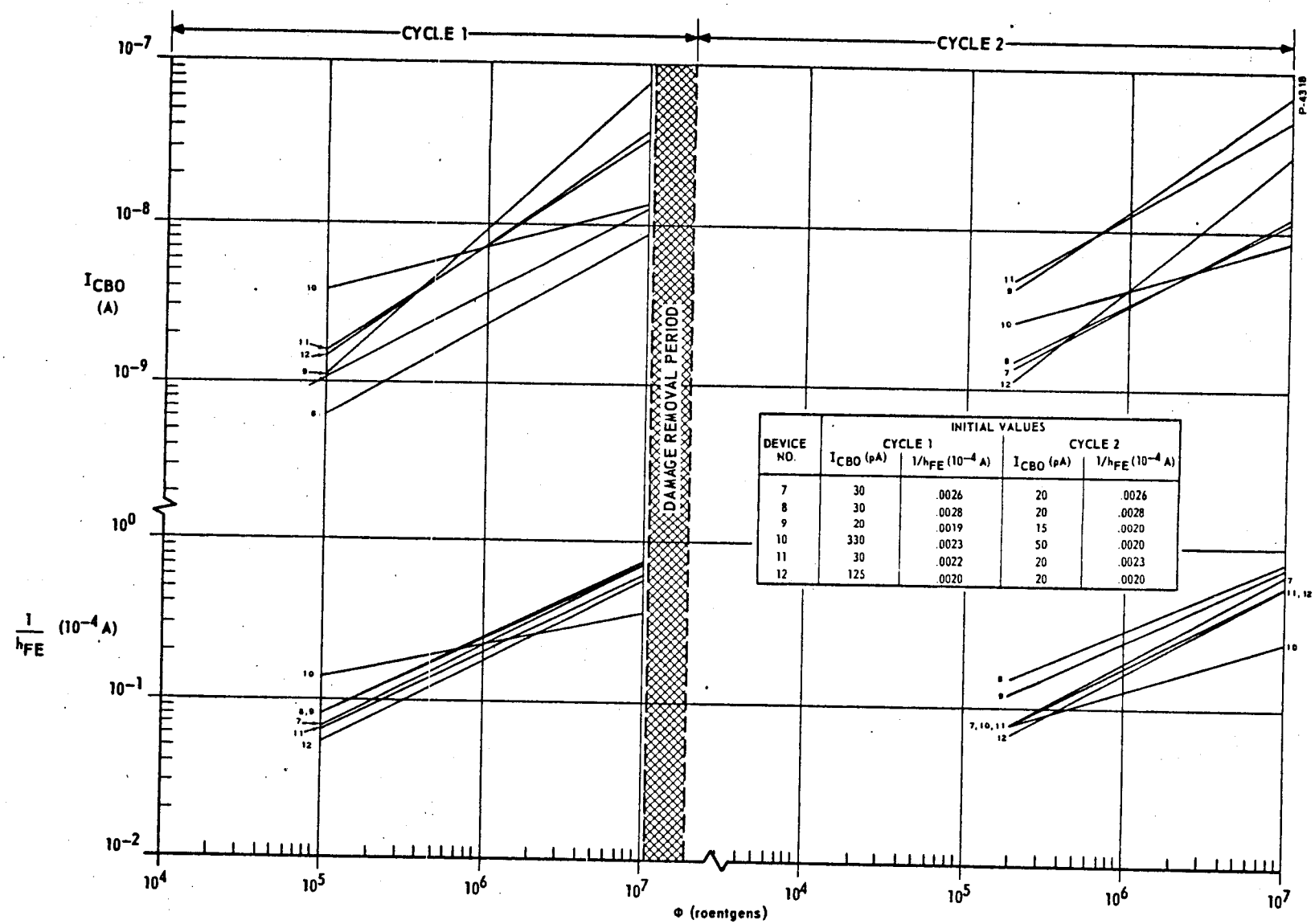


Figure 6-8 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, Westinghouse 2N3058 (p-n-p)



DEVICE NO.	INITIAL VALUES CYCLE 1 I_{CBO} (pA)	CYCLE 1 $1/h_{FE}$ (10^{-4} A)	CYCLE 2 I_{CBO} (pA)	CYCLE 2 $1/h_{FE}$ (10^{-4} A)
1	30	.0017	42000	.0017
2	40	.0026	22000	.0028
3	30	.0040	32000	.0047
4	30	.0033	98000	.0036
5	20	.0021	HIGH	.0021
6	30	.0023	50	.0024

Figure 6-9 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, Crystalonics 2N3964 (p-n-p)



DEVICE NO.	INITIAL VALUES CYCLE 1 I_{CBO} (pA)	CYCLE 1 $1/h_{FE}$ (10^{-4} A)	CYCLE 2 I_{CBO} (pA)	CYCLE 2 $1/h_{FE}$ (10^{-4} A)
7	30	.0026	20	.0026
8	30	.0028	20	.0028
9	20	.0019	15	.0020
10	330	.0023	50	.0020
11	30	.0022	20	.0023
12	125	.0020	20	.0020

Figure 6-10 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, Fairchild 2N3964 (p-n-p)

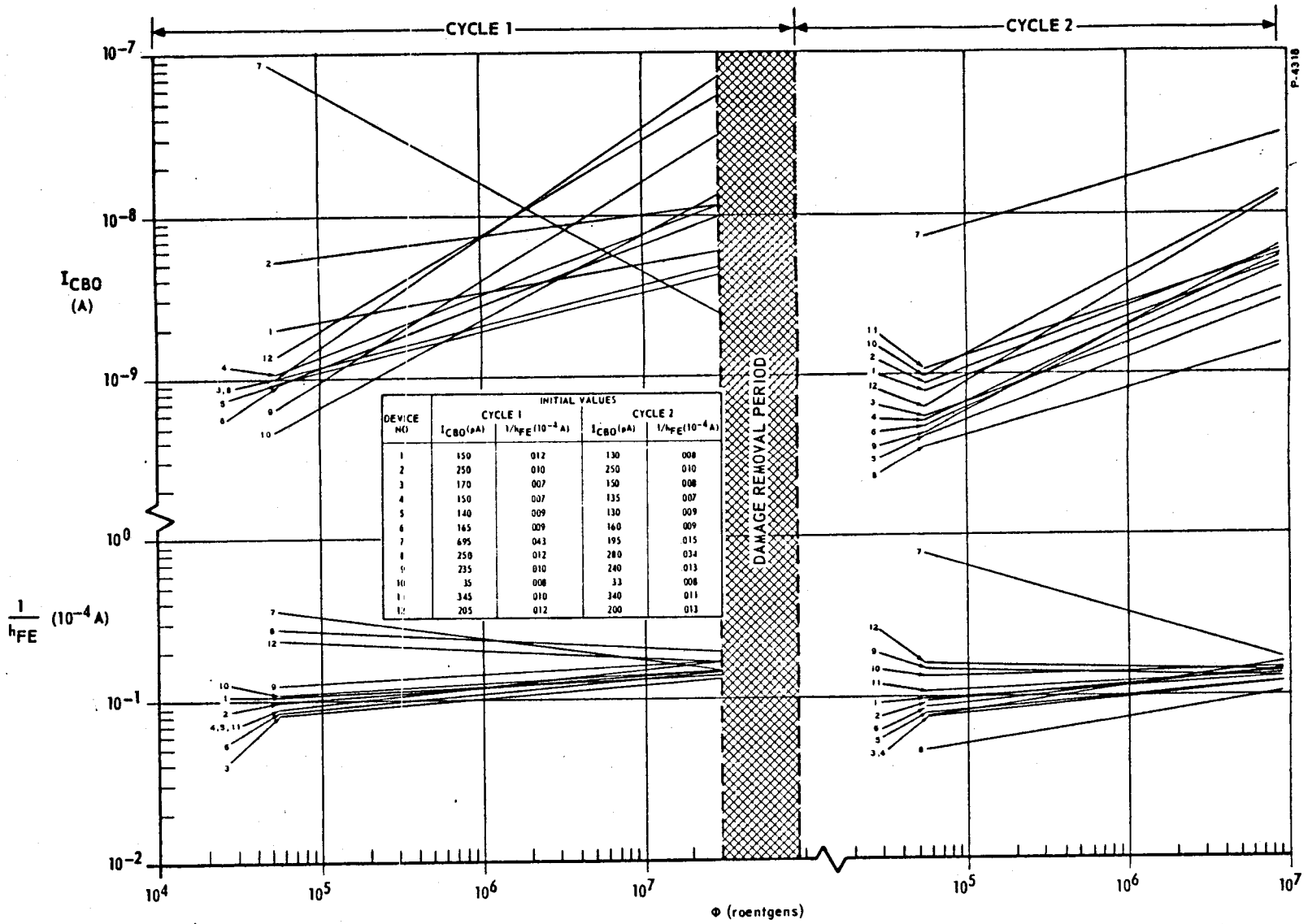


Figure 6-11 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, Motorola 2N2219A

DEVICE NO.	INITIAL VALUES CYCLE 1 I_{CBO} (pA)	CYCLE 1 $1/h_{FE}$ (10^{-4})	CYCLE 2 I_{CBO} (pA)	CYCLE 2 $1/h_{FE}$ (10^{-4})	CYCLE 3 I_{CBO} (pA)	CYCLE 3 $1/h_{FE}$ (10^{-4})
1	.5	.0027	5	.0064	<5	.0075
2	.5	.0026	5	.0054	<5	.0069
3	20	.0043				
4	.5	.0029				
5	20	.0029	<5	.0028	<5	.0031
6	20	.0032				
7	<5	.0019	<5	.0021	<5	.0026
8	10	.0022	<5	.0014	<5	.0011
9	15	.0025	<5	.0029	<5	.0035
10	20	.0030	<5	.0094	<5	.0053
11	10	.0033	<5	.0022	<5	.0027
12	6400	.0034	11900	.0078		

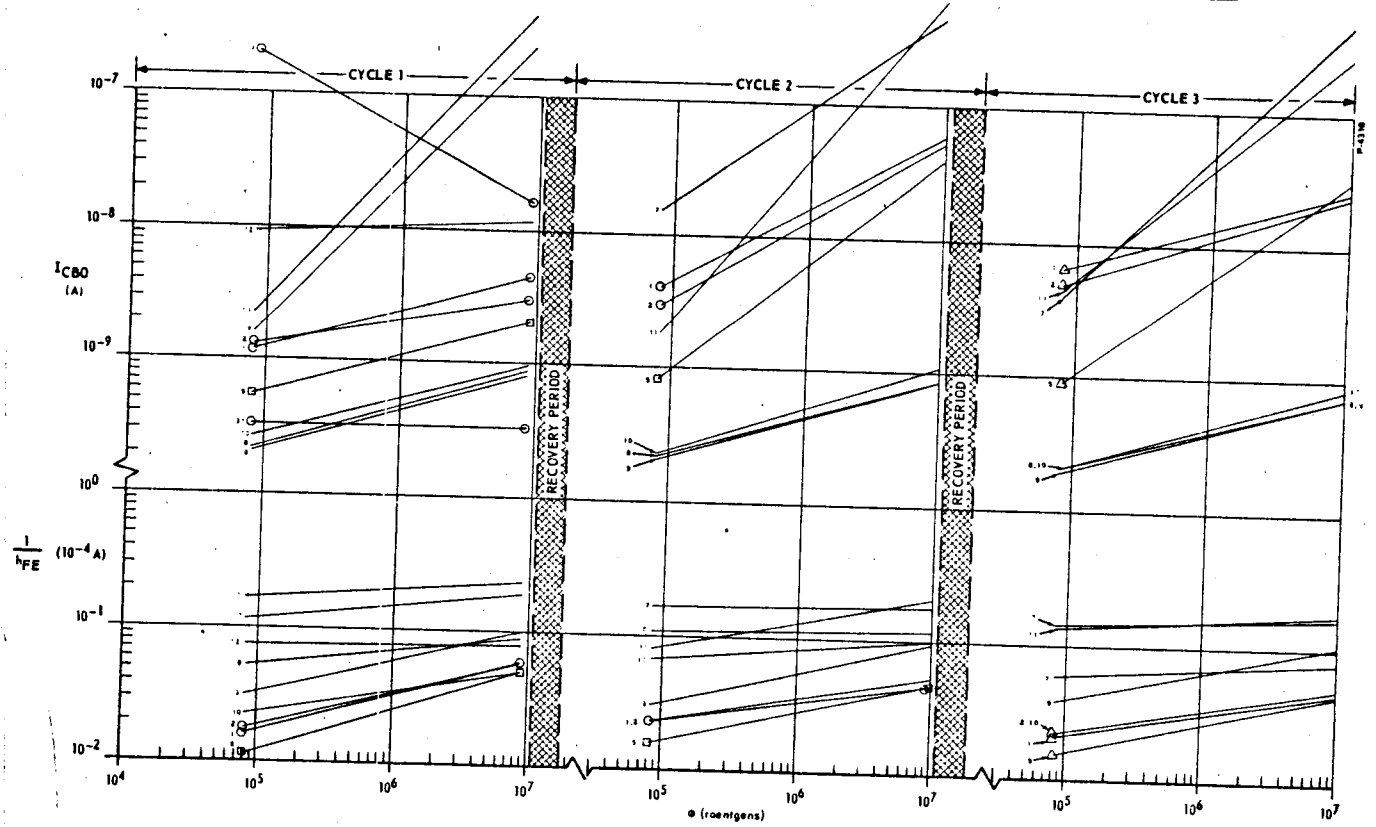


Figure 6-12 - Spreads of $1/h_{FE}$ and I_{CBO} versus ϕ characteristics for two cycles of irradiation, Fairchild TD106 (n-p-n)

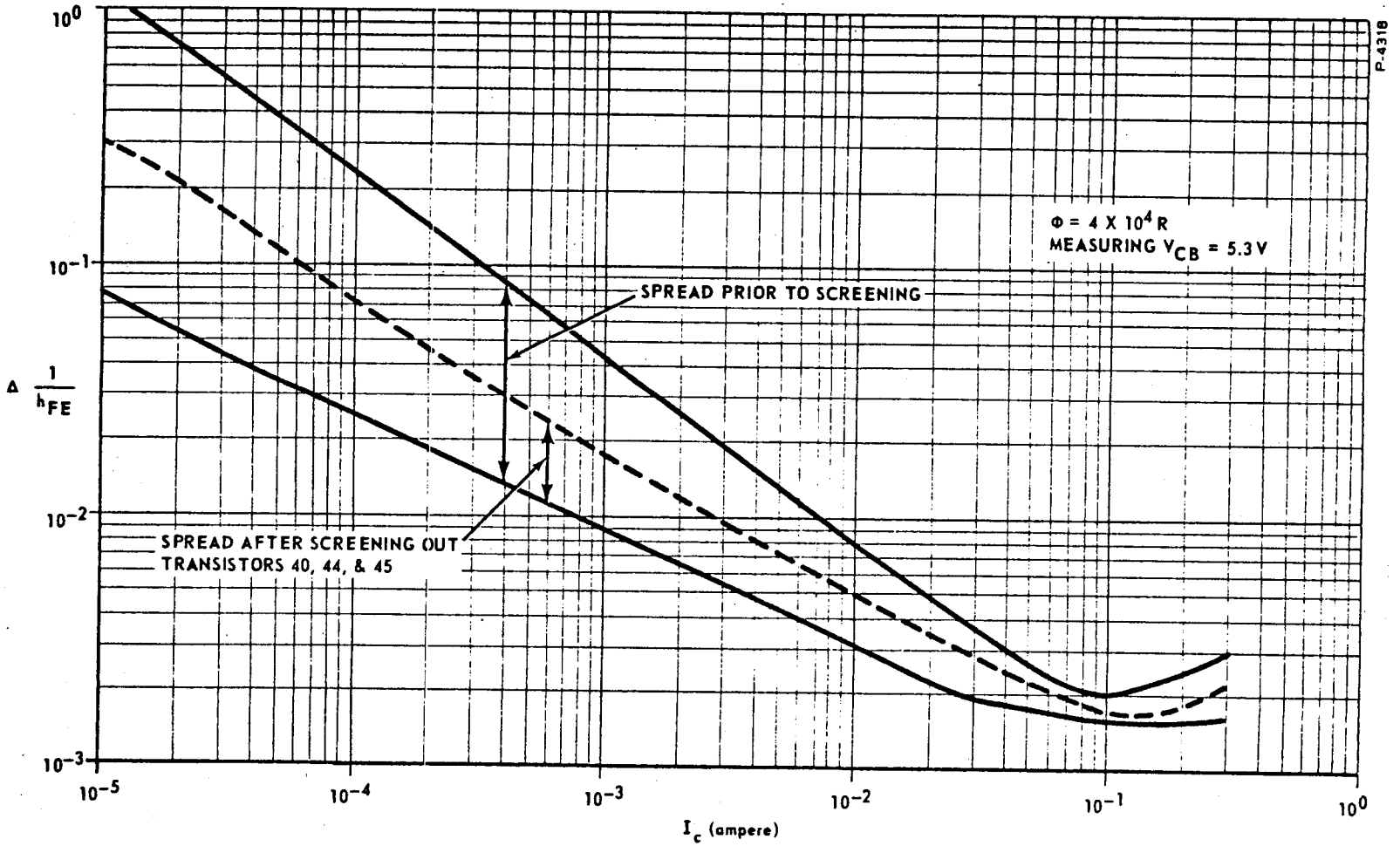


Figure 6-13 - Spreads of $\Delta \frac{1}{h_{FE}}$ versus I_C characteristics after small dose, before and after screening, 2N1613

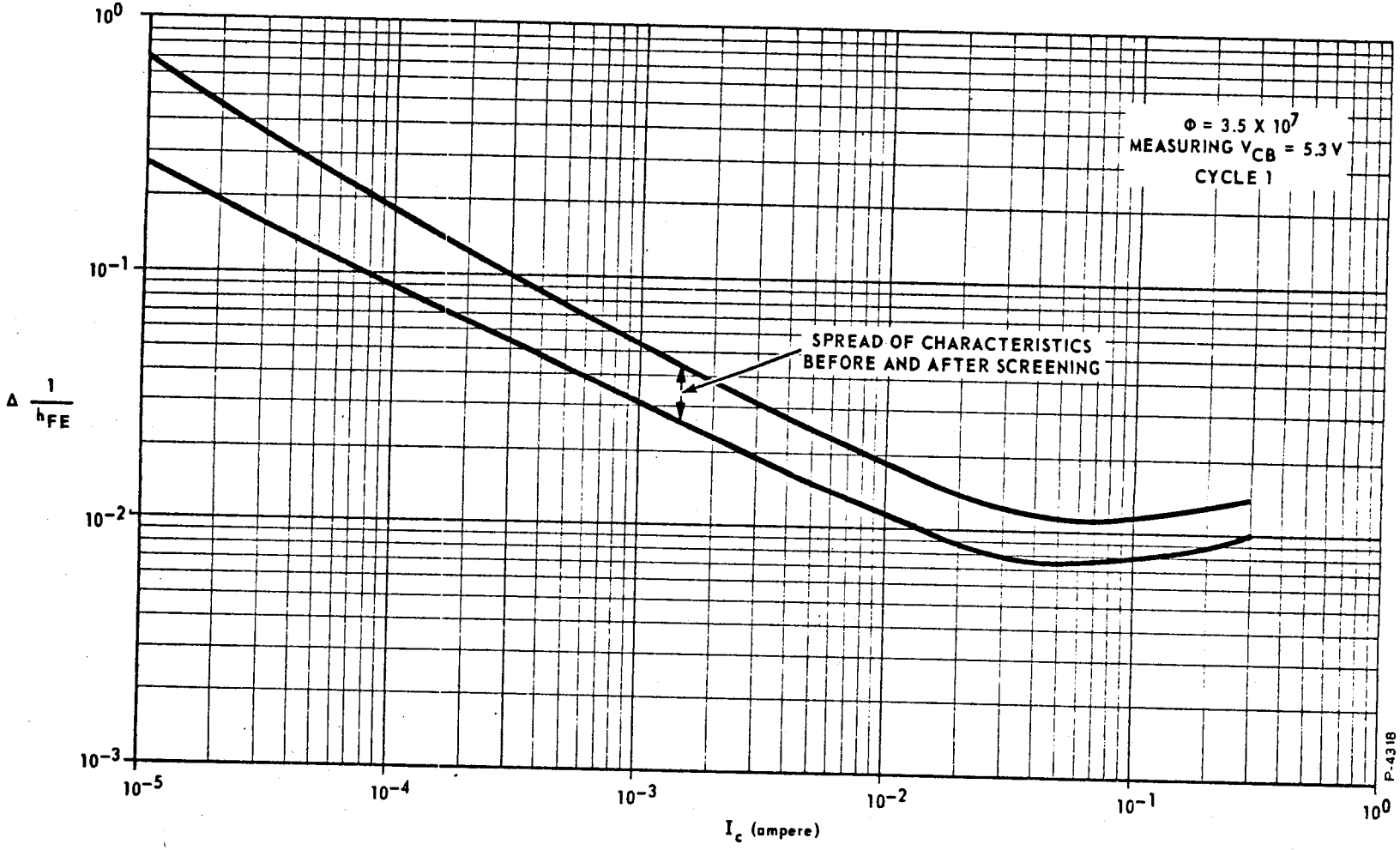


Figure 6-14 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after large dose, before and after screening, 2N1613

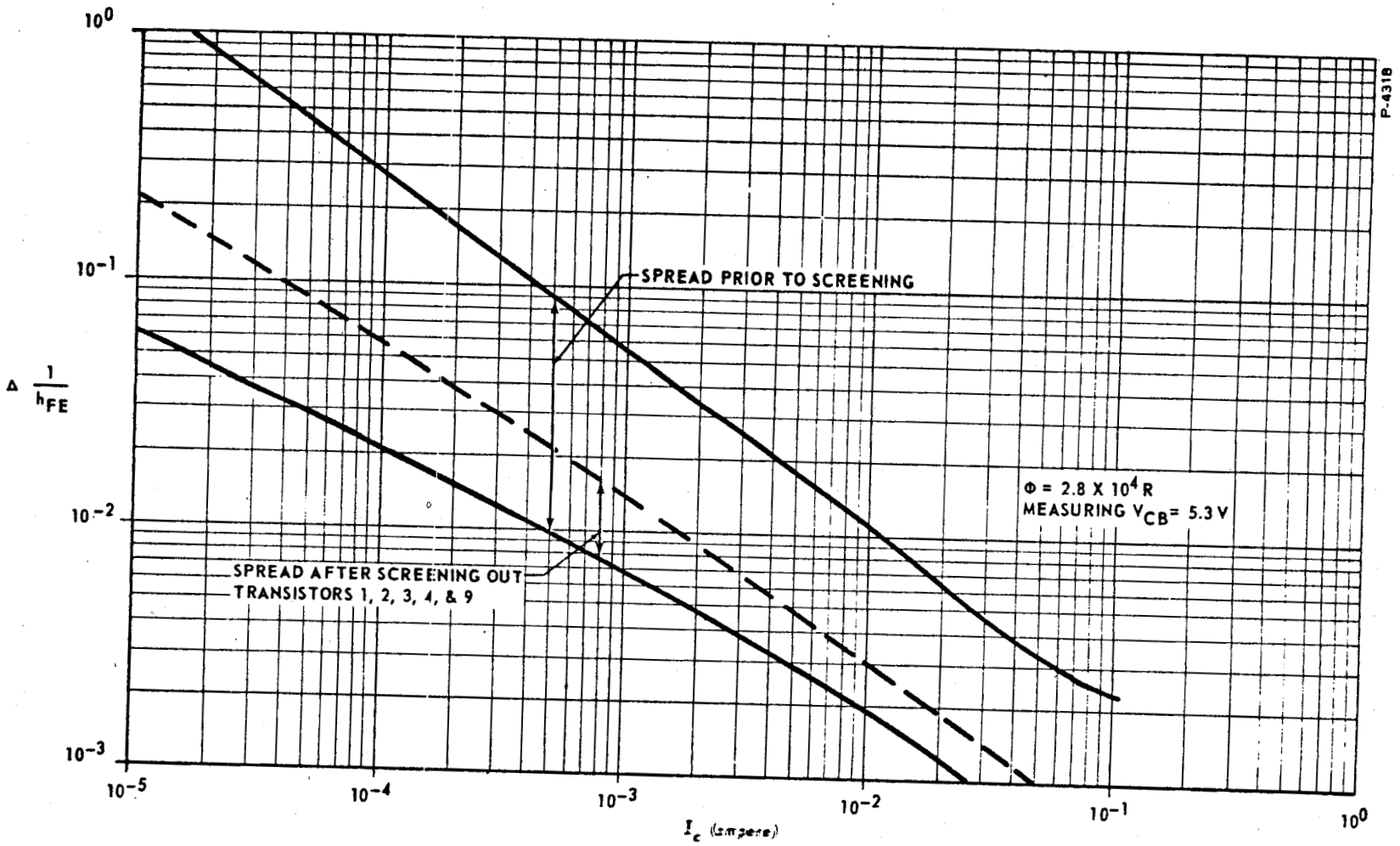


Figure 6-15 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after small dose, before and after screening, Motorola 2N2222

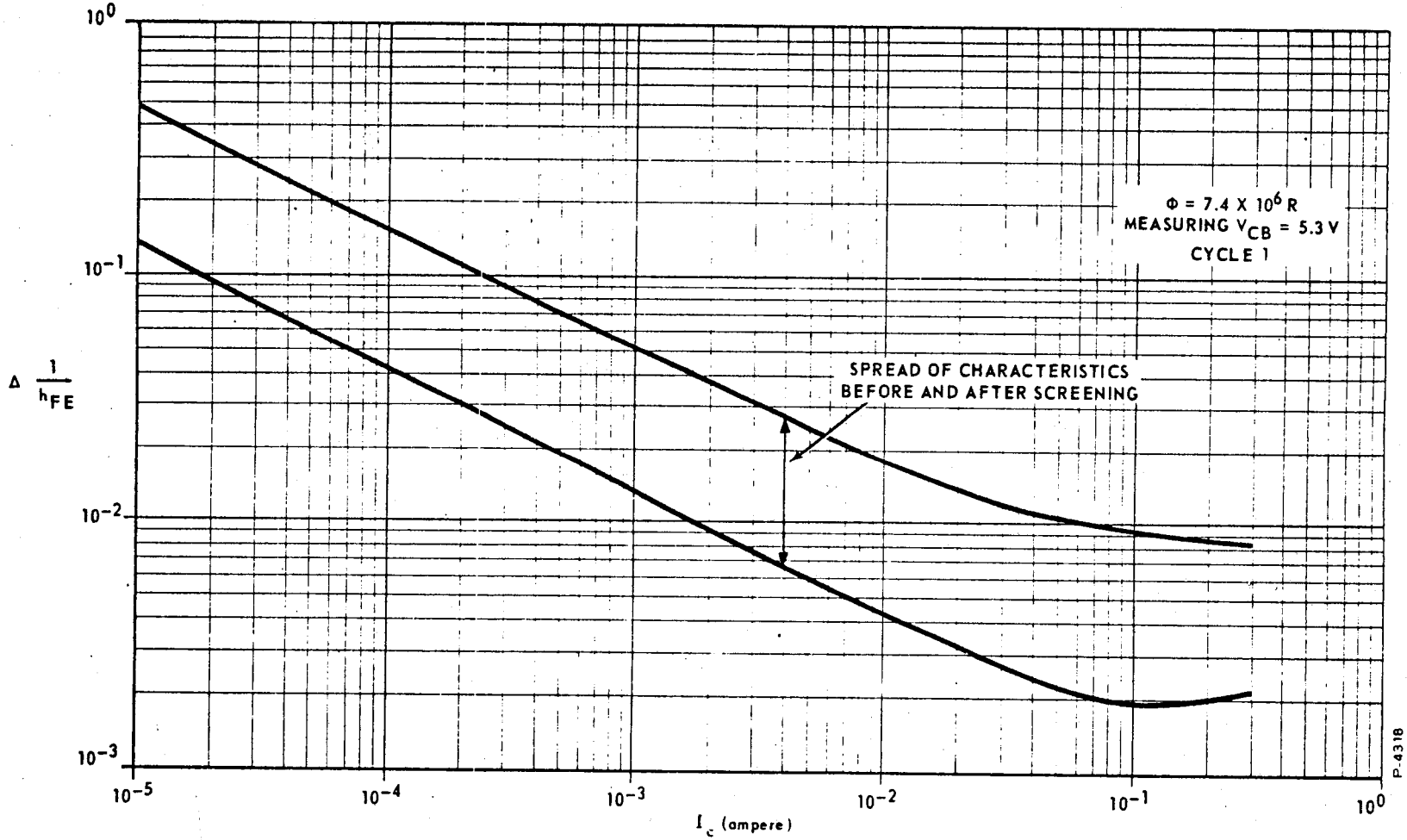


Figure 6-16 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after large dose, before and after screening, Motorola 2N2222

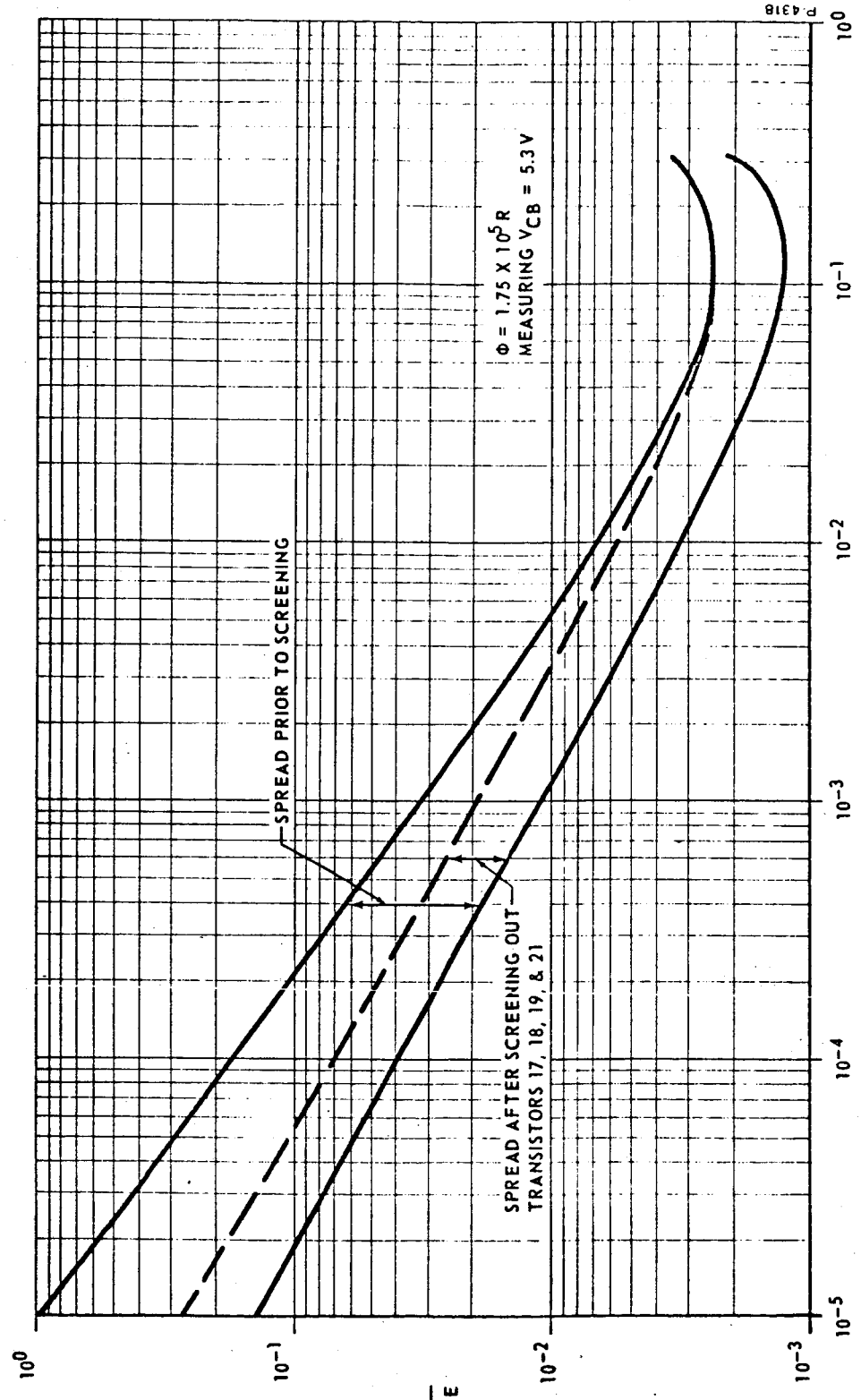


Figure 6-17 - Spreads of $\Delta \frac{1}{h_{FE}}$ versus I_C characteristics after small dose, before and after screening, Fairchild 2N2222

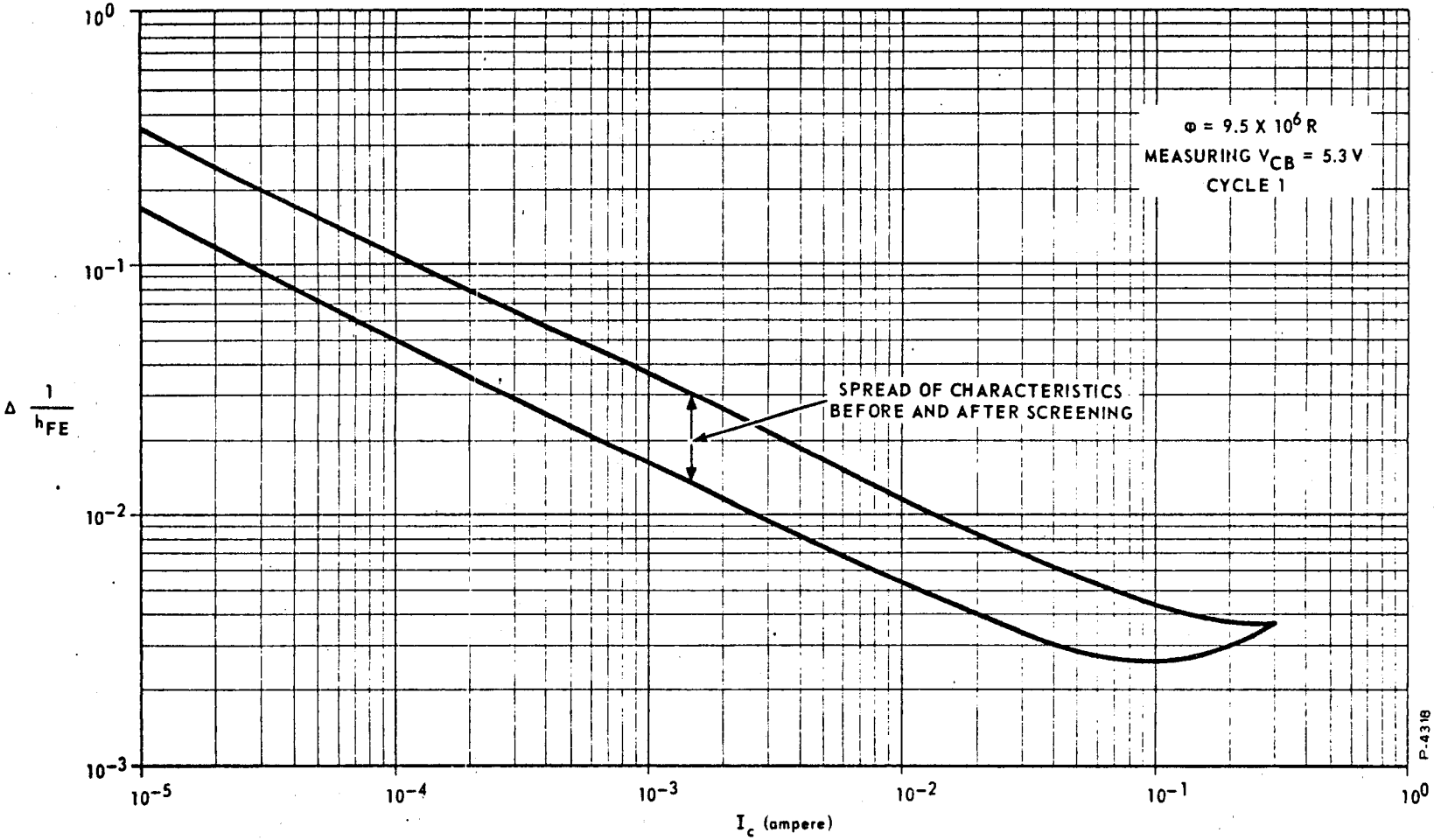


Figure 6-18 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after large dose, before and after screening, Fairchild 2N2222

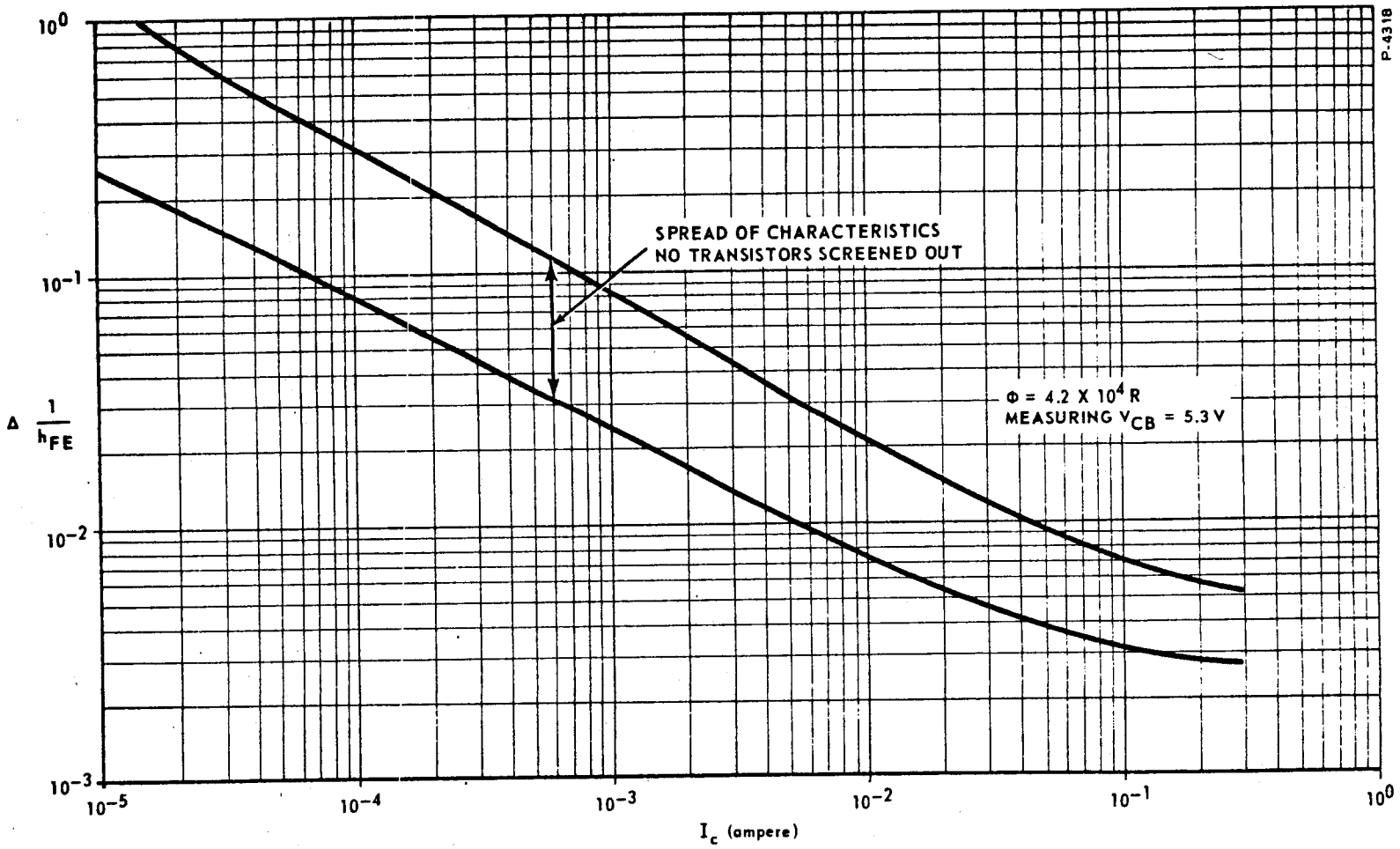


Figure 6-19 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after small dose, before and after screening, Motorola 2N2905

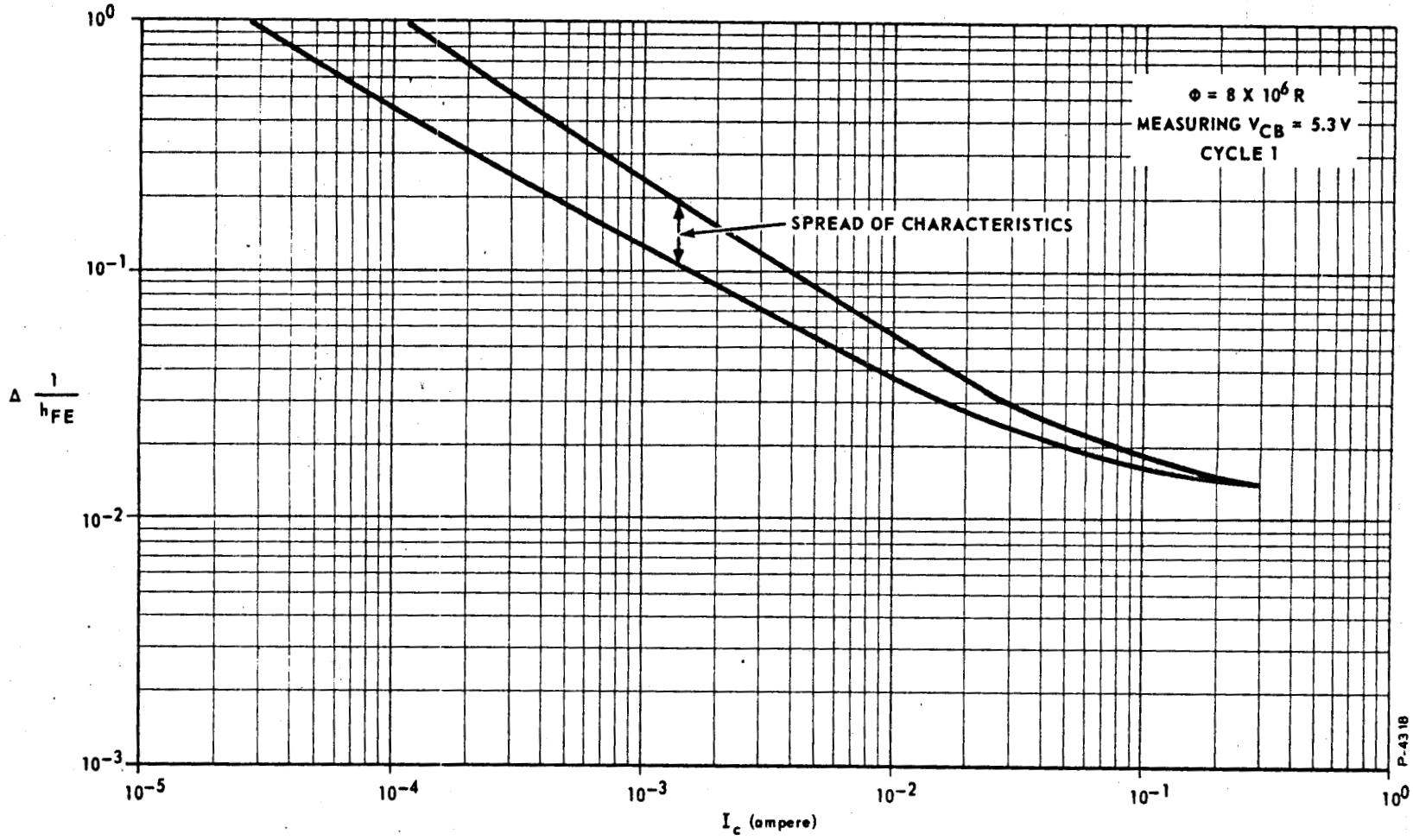


Figure 6-20 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after large dose, before and after screening, Motorola 2N2905

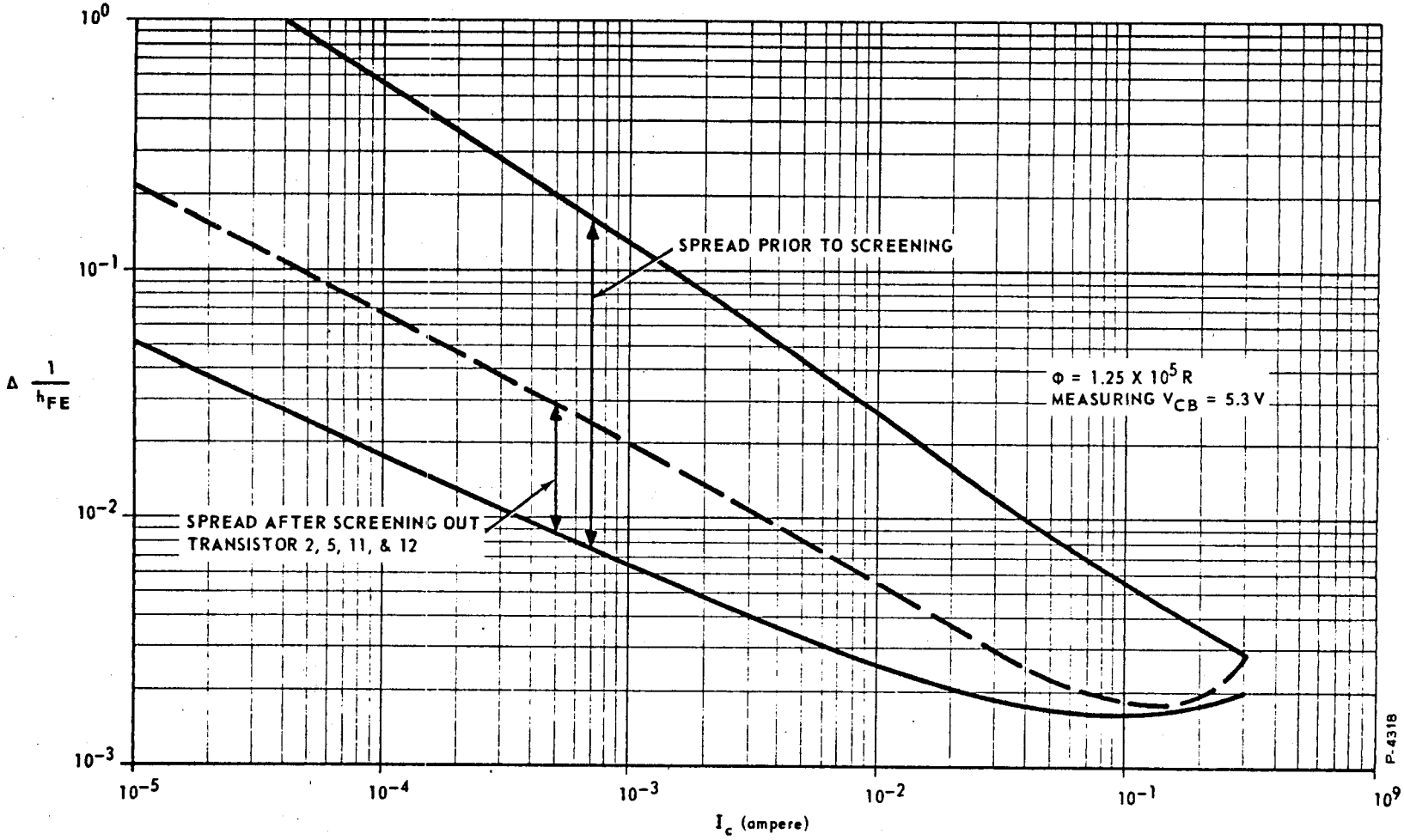


Figure 6-21 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after small dose, before and after screening, Texas Instruments 2N1132

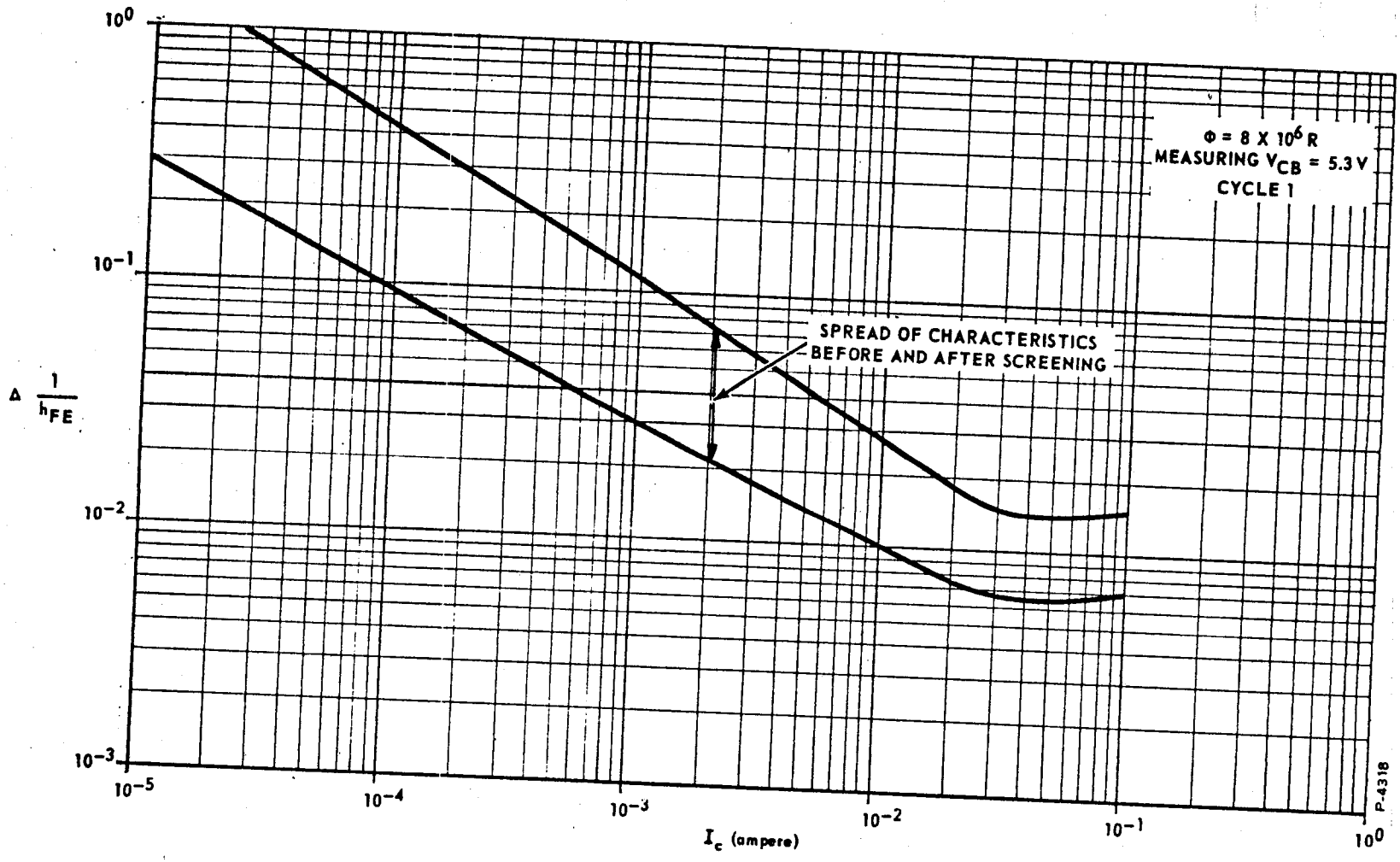


Figure 6-22 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after large dose, before and after screening, Texas Instruments 2N1132

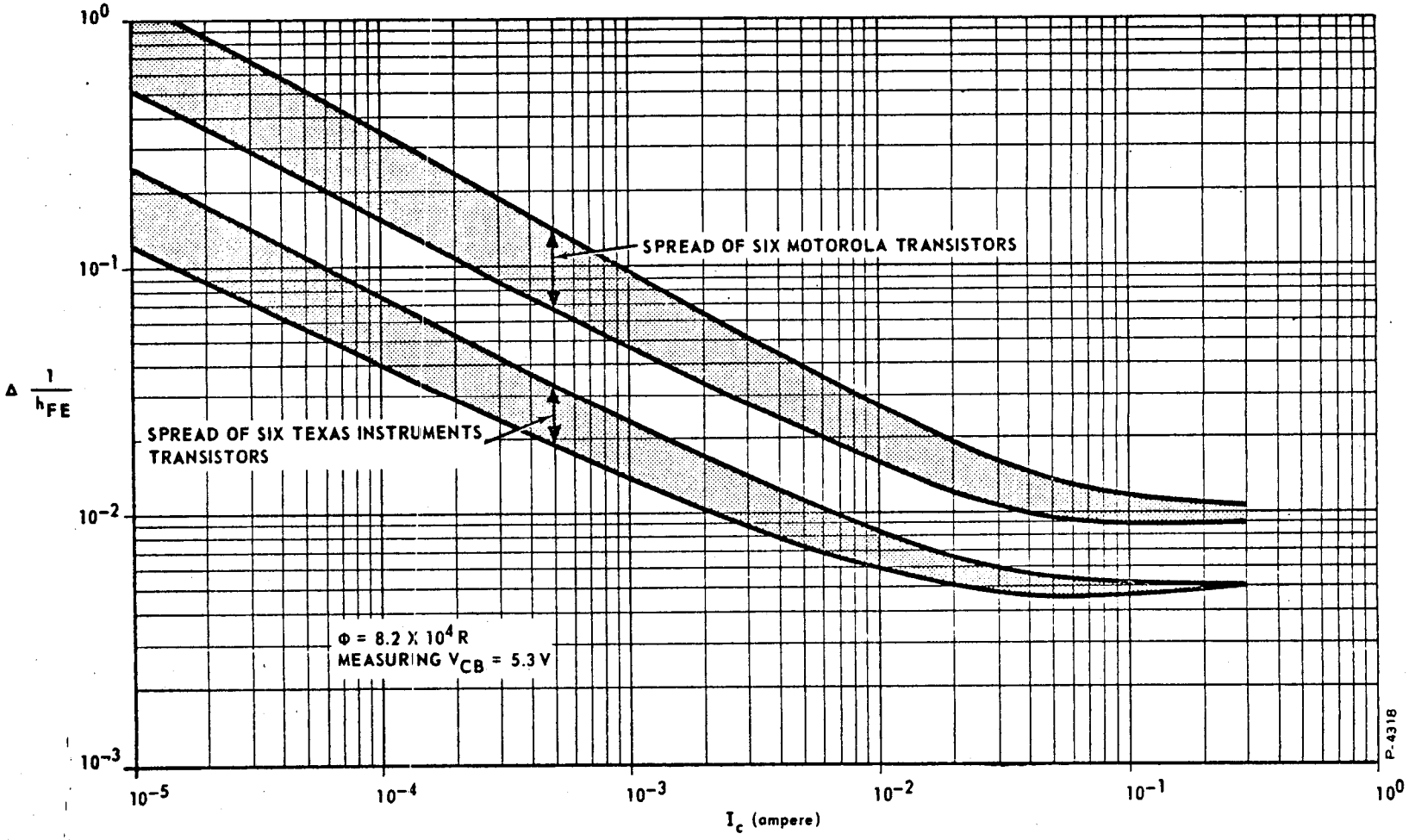


Figure 6-23 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after small dose, before and after screening, 2N722, Texas Instruments 1-6, Motorola 7-12

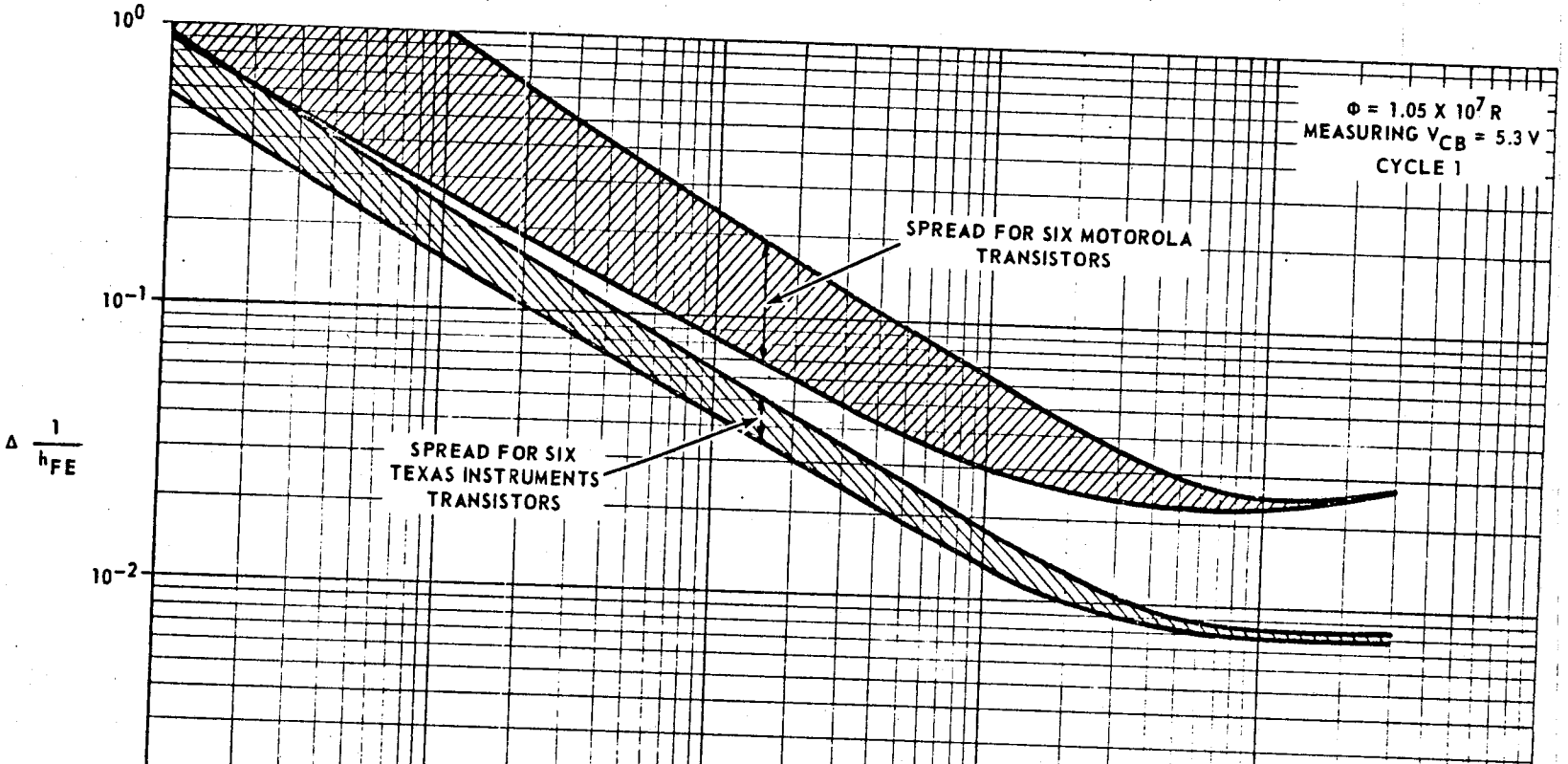


Figure 6-24 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after large dose, before and after screening, 2N722, Texas Instruments 1-6, Motorola 7-12

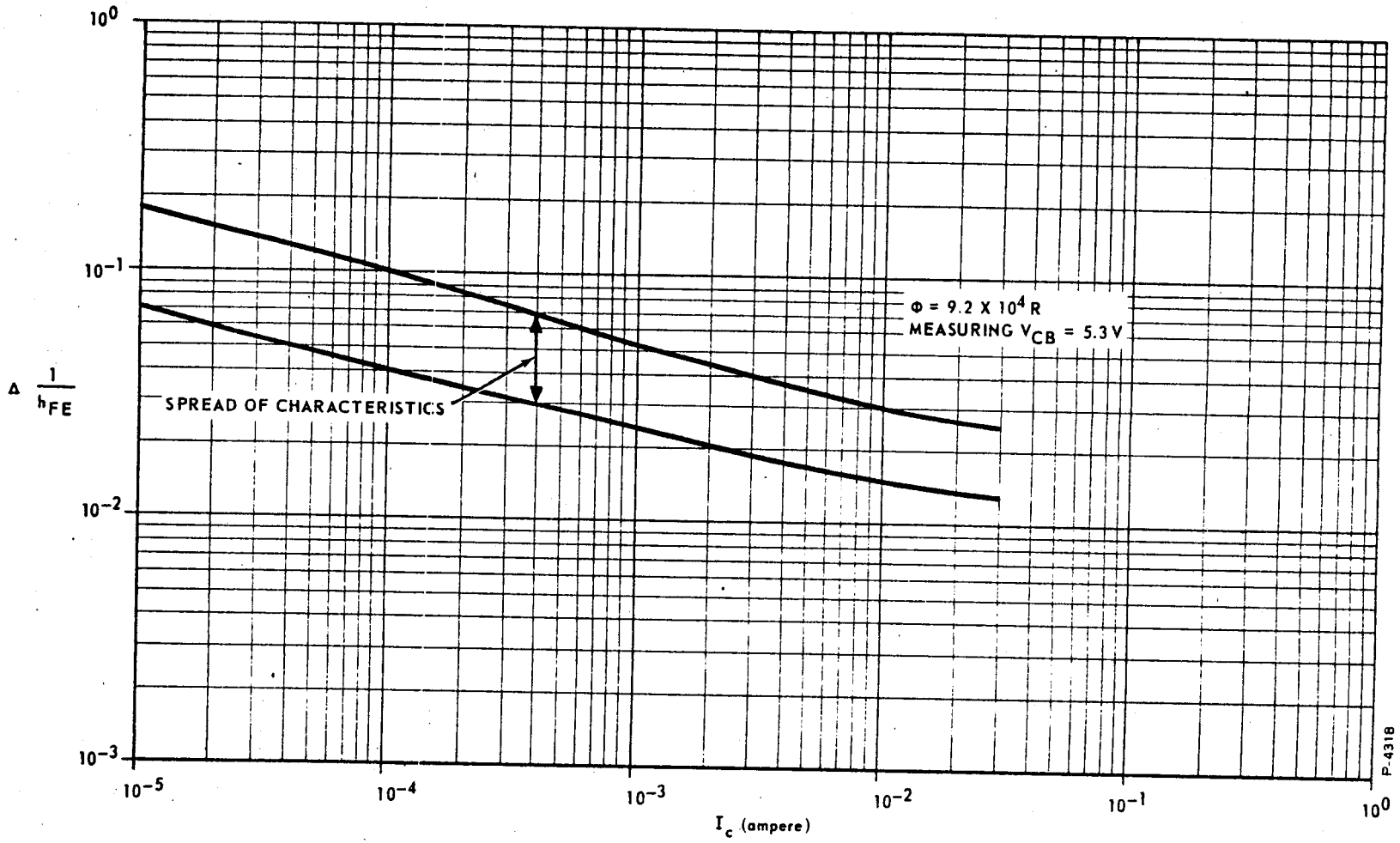


Figure 6-25 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after small dose, before and after screening, Crystalonics 2N3058

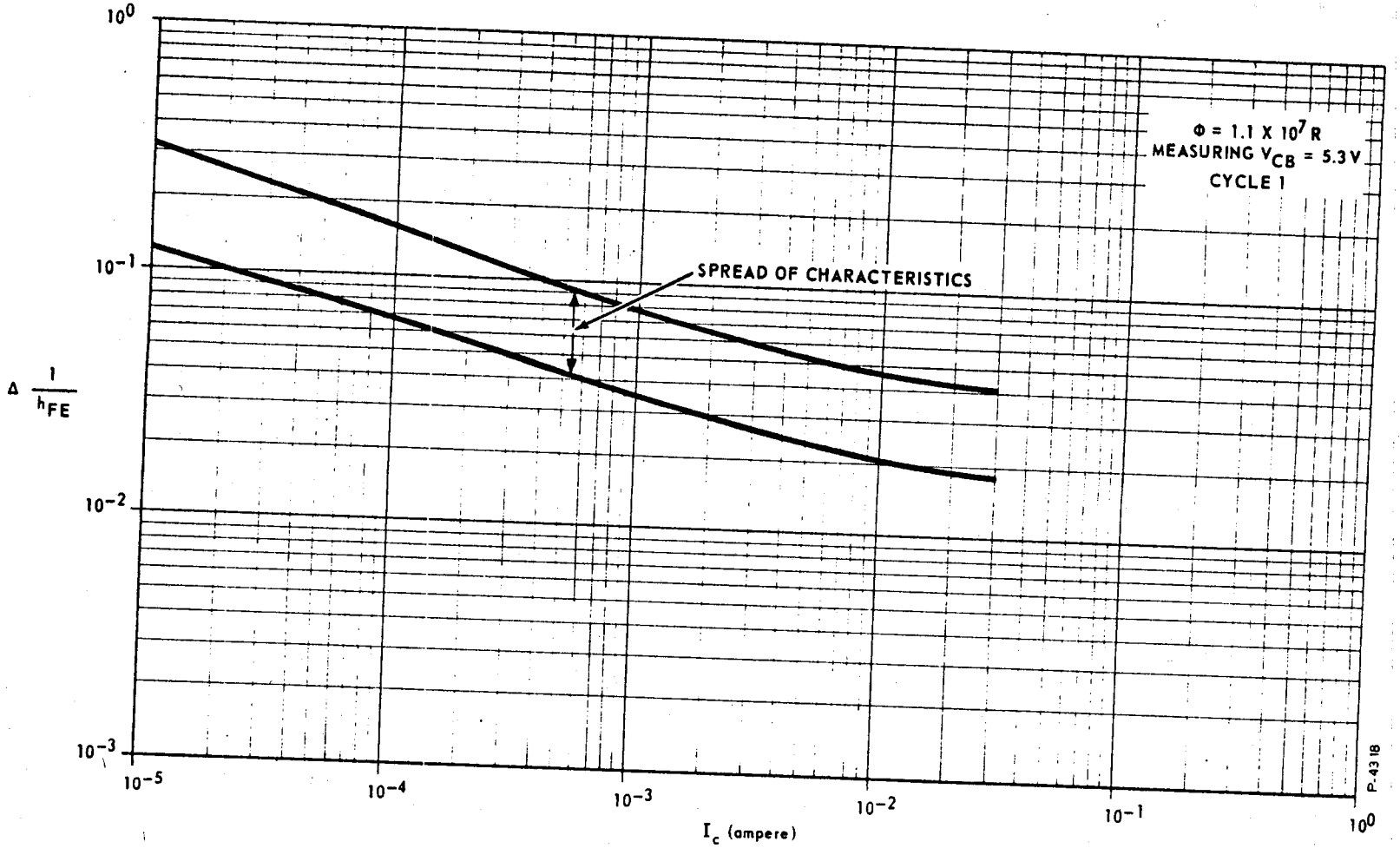


Figure 6-26 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after large dose, before and after screening, Crystalonics 2N3058

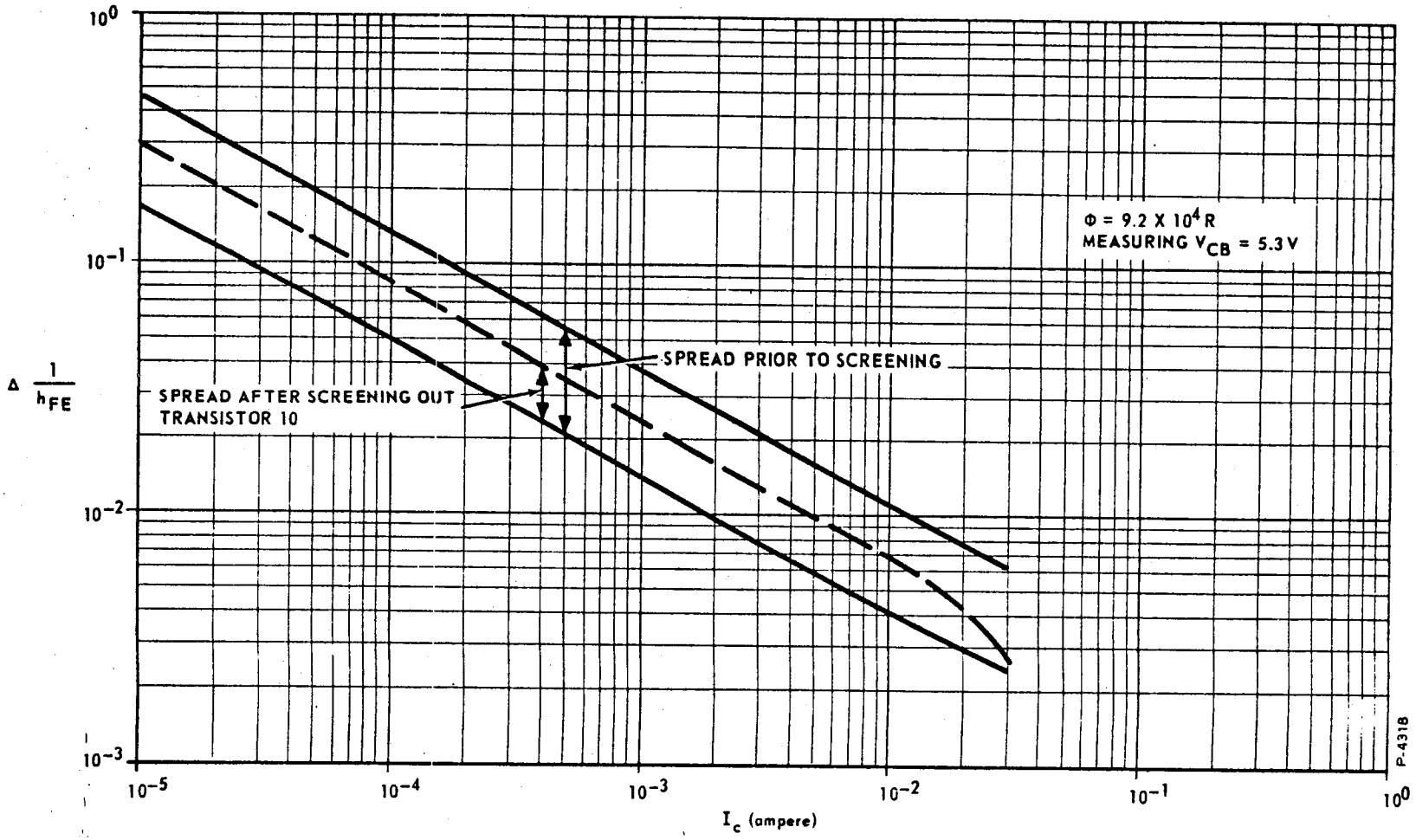


Figure 6-27 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after small dose, before and after screening, Fairchild 2N3964

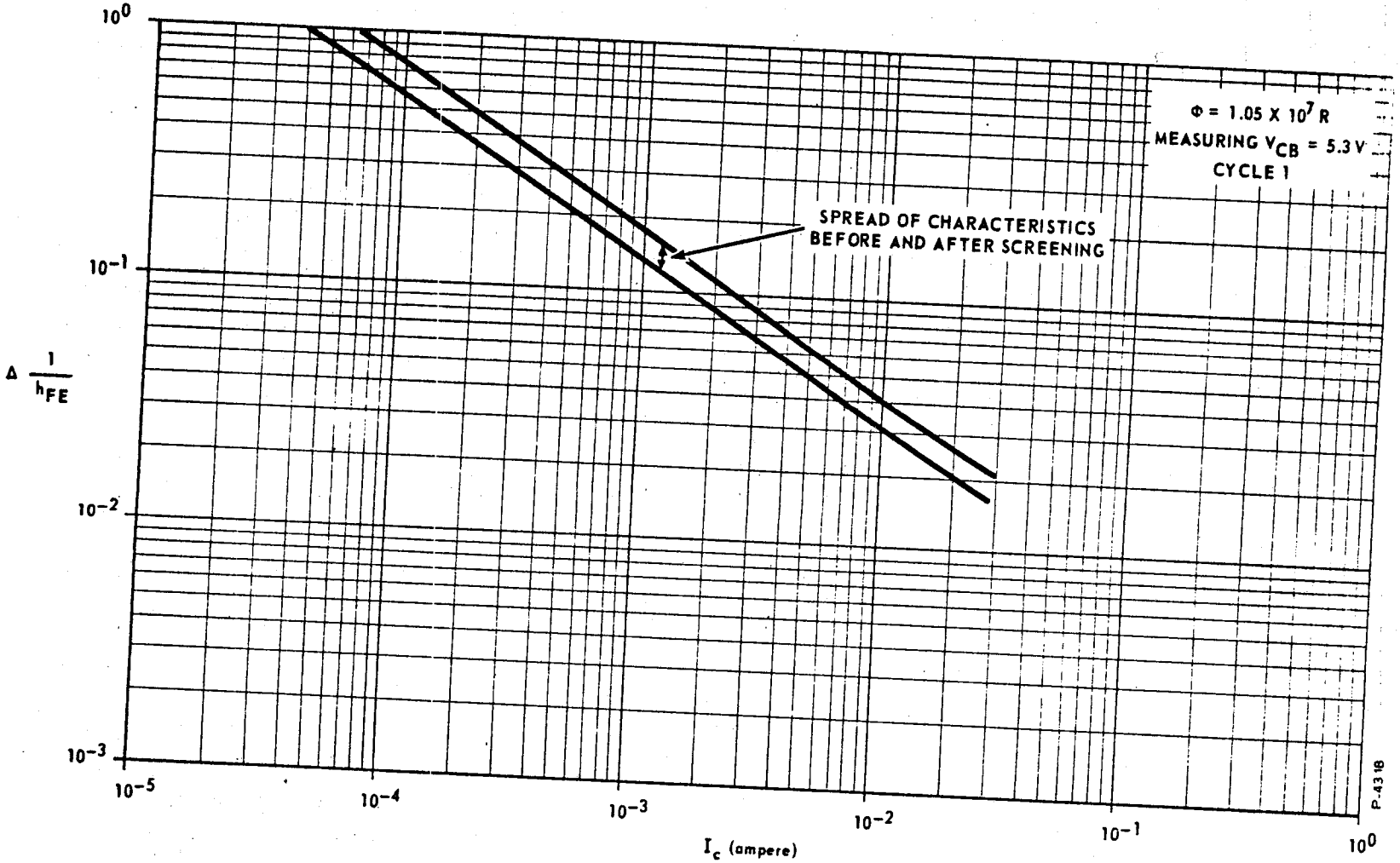


Figure 6-28 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after large dose, before and after screening, Fairchild 2N3964

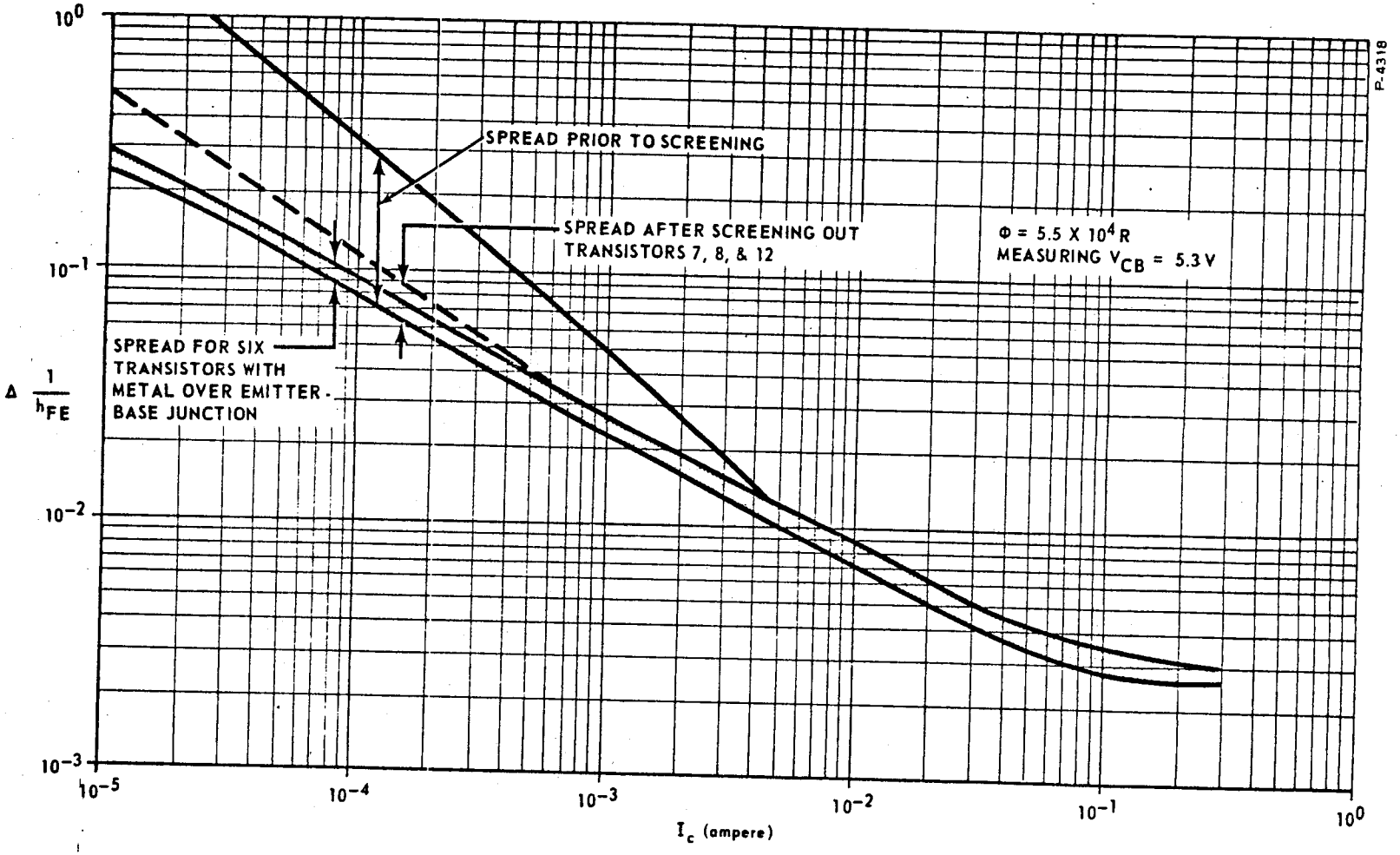


Figure 6-29 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after small dose, before and after screening, Motorola 2N2219A

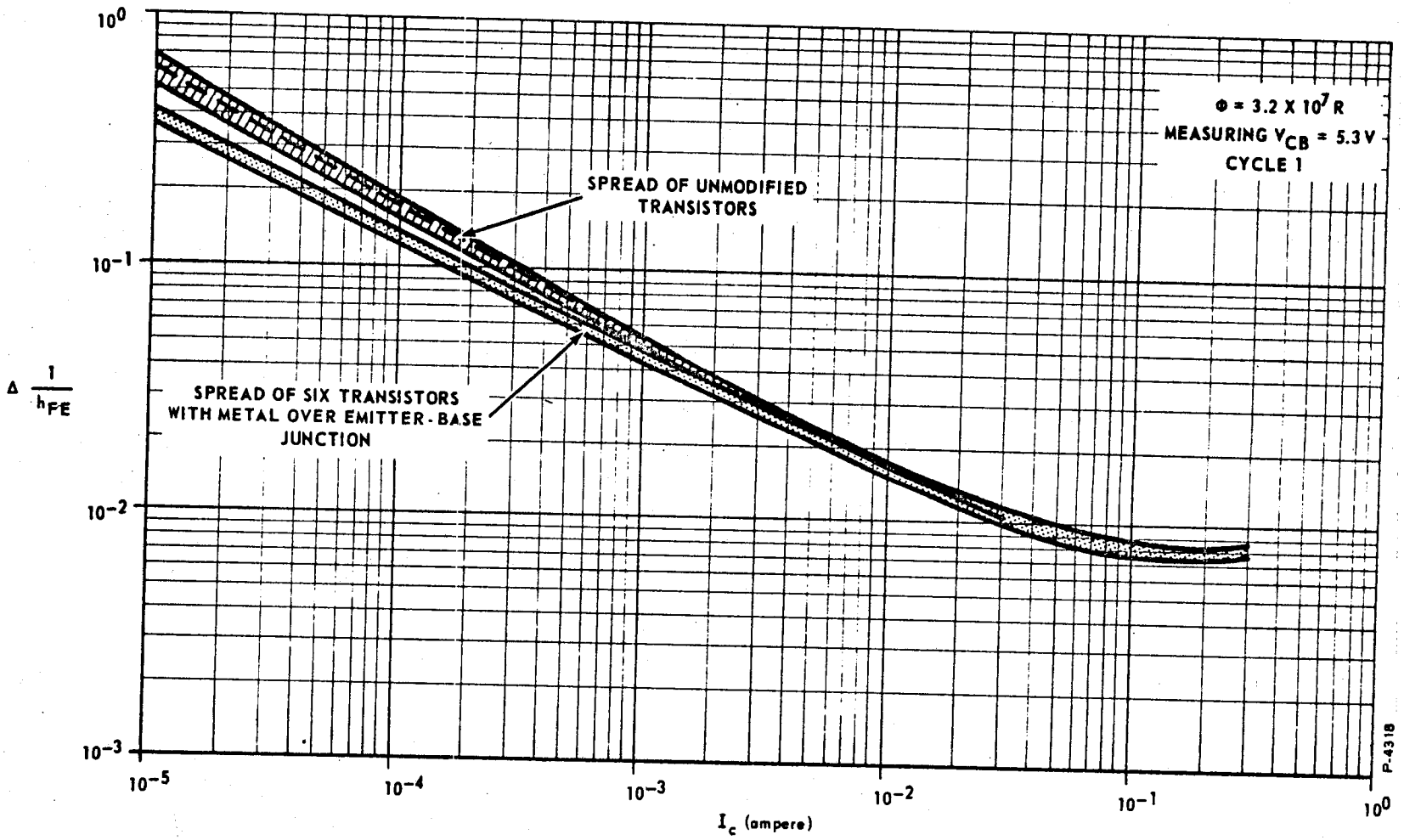


Figure 6-30 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after large dose, before and after screening, Motorola 2N2219A

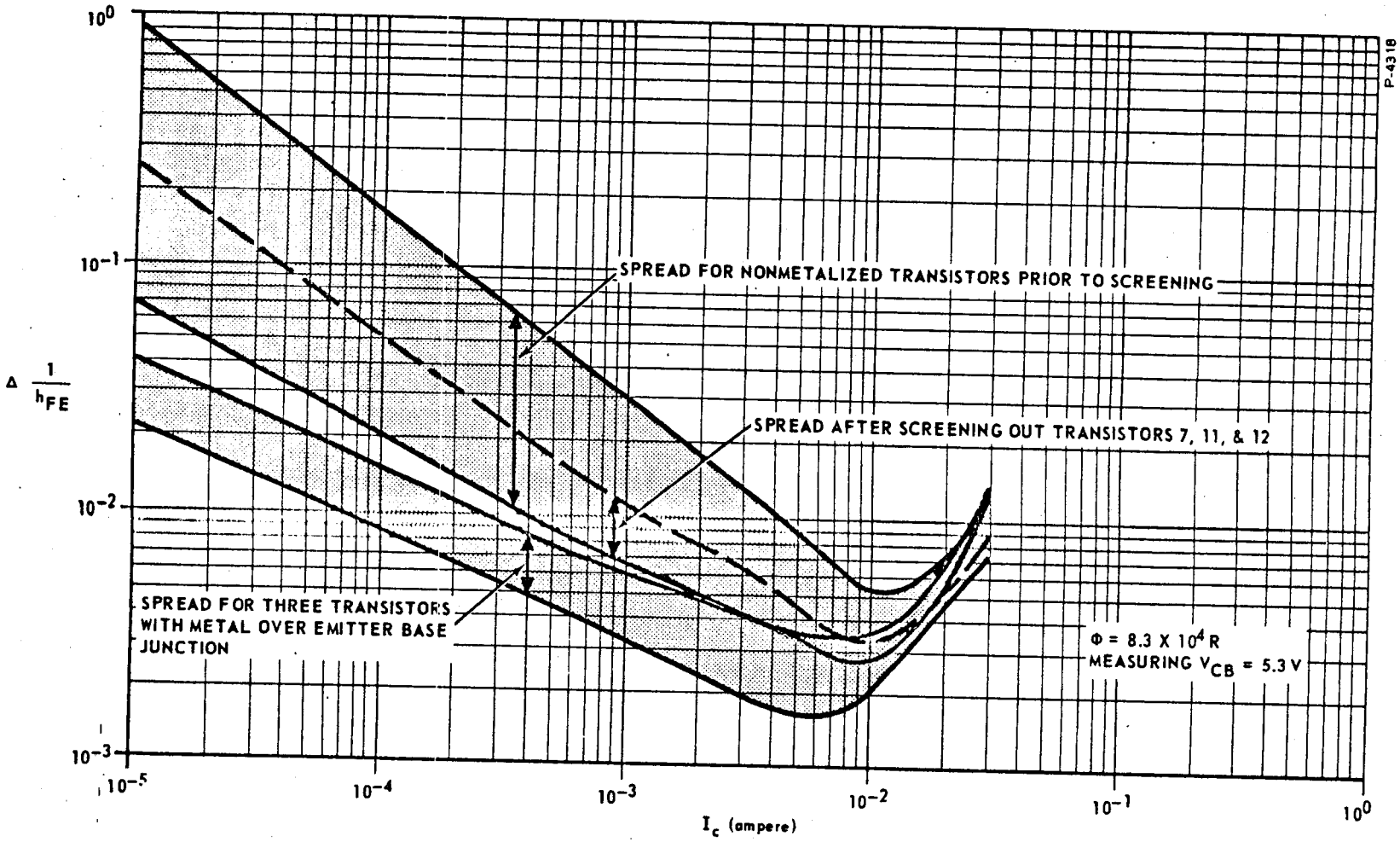


Figure 6-31 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after small dose, before and after screening, Fairchild TD106, 1-6 metallized, 7-12 nonmetallized

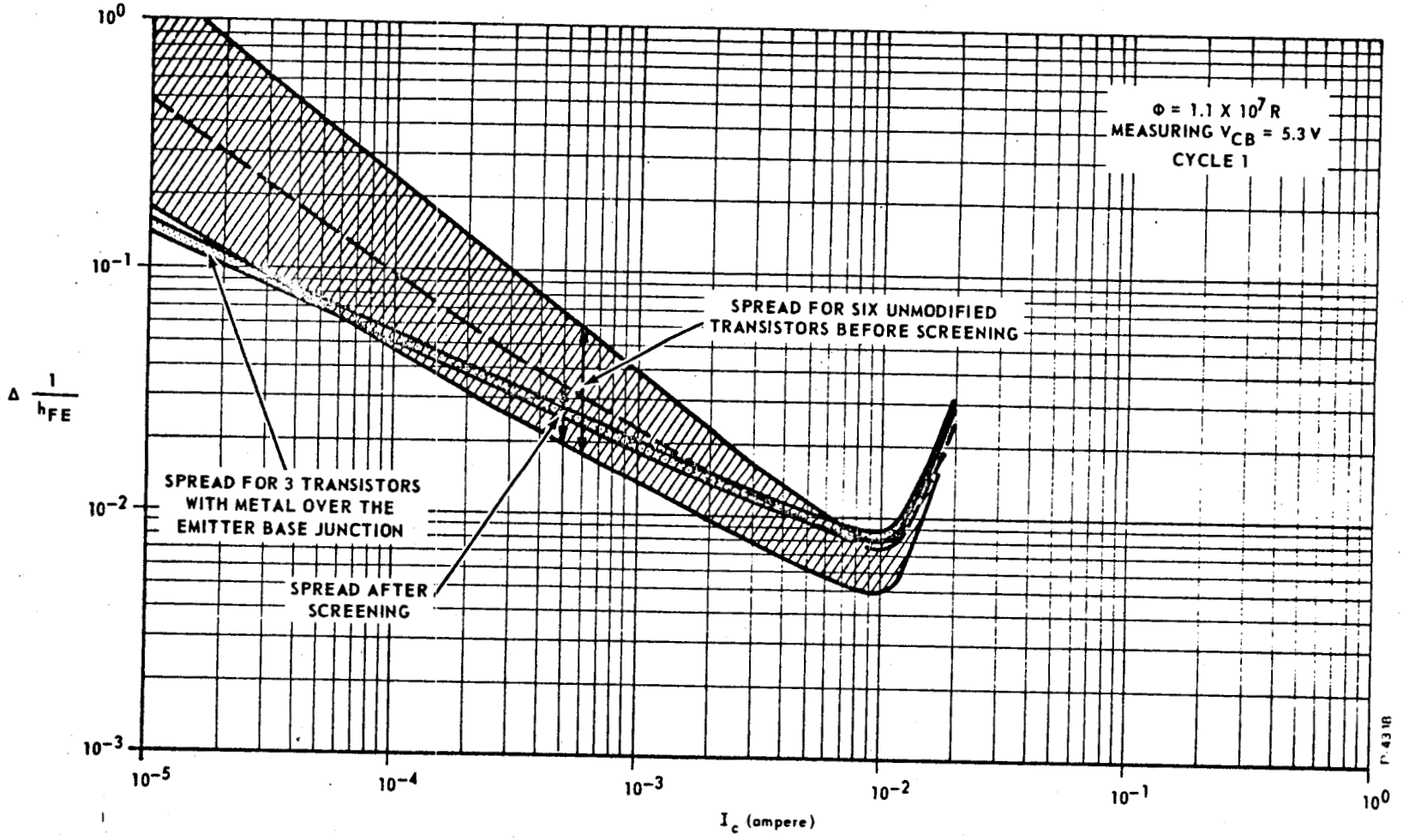


Figure 6-32 - Spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics after large dose, before and after screening, Fairchild TD106, 1-6 metallized, 7-12 nonmetallized

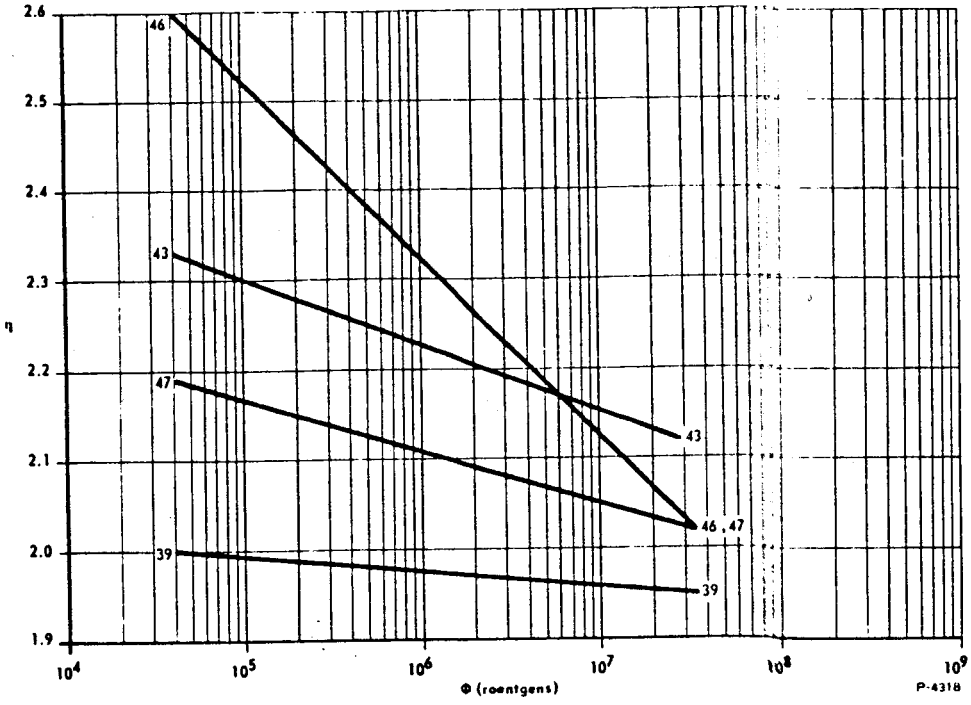


Figure 6-33 - n versus ϕ, Fairchild 2N1613

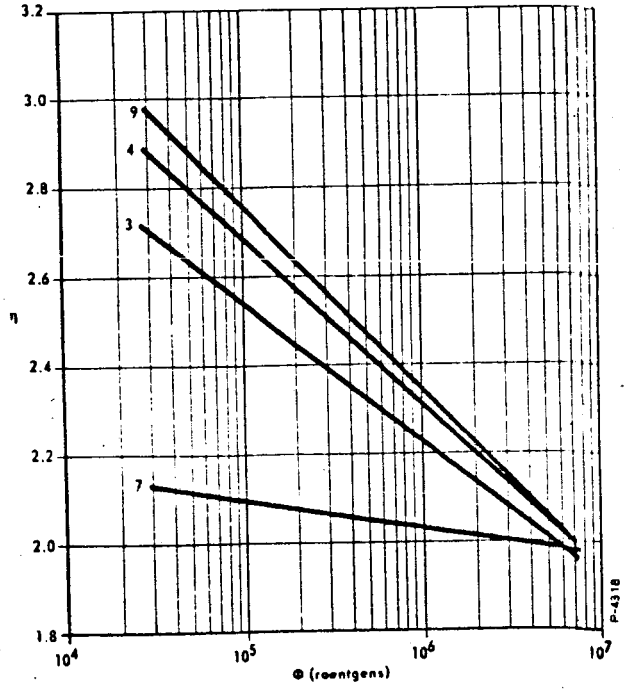


Figure 6-34 - n versus ϕ, Motorola 2N2222

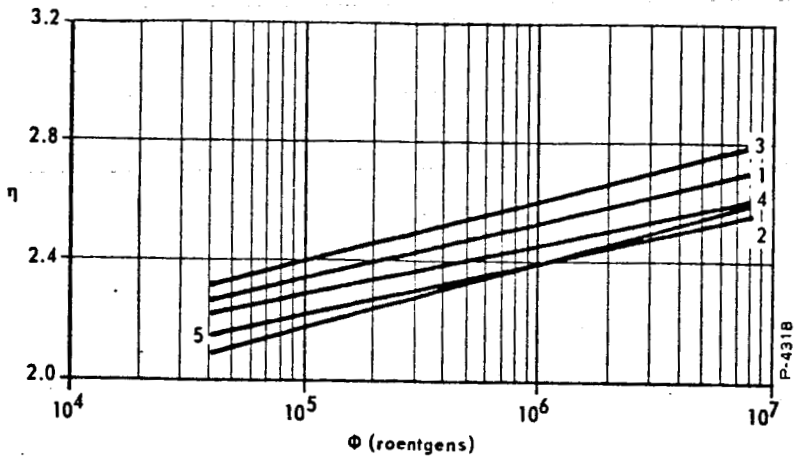


Figure 6-35 - n versus ϕ, Motorola 2N2905

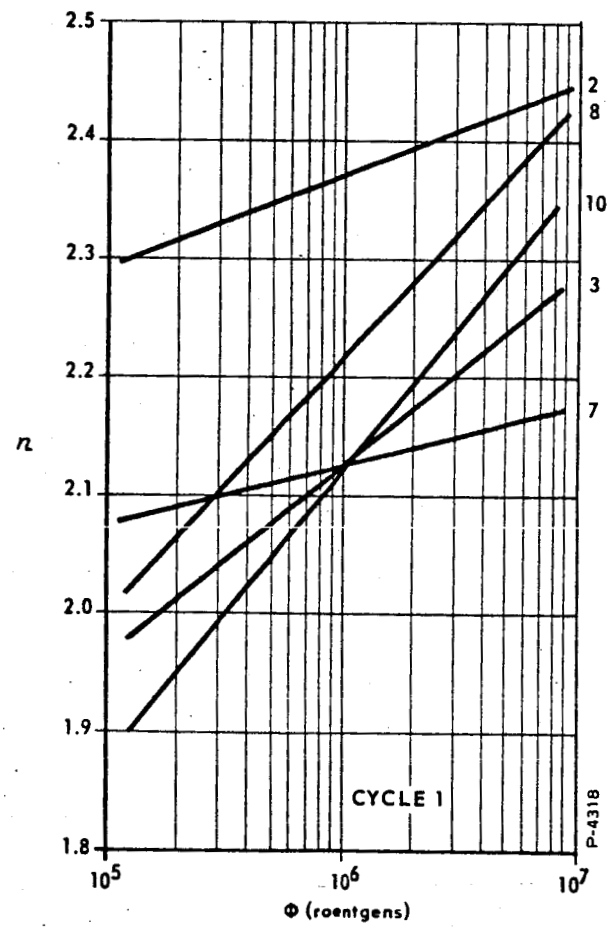


Figure 6-36 - n versus ϕ, Texas Instruments 2N1132

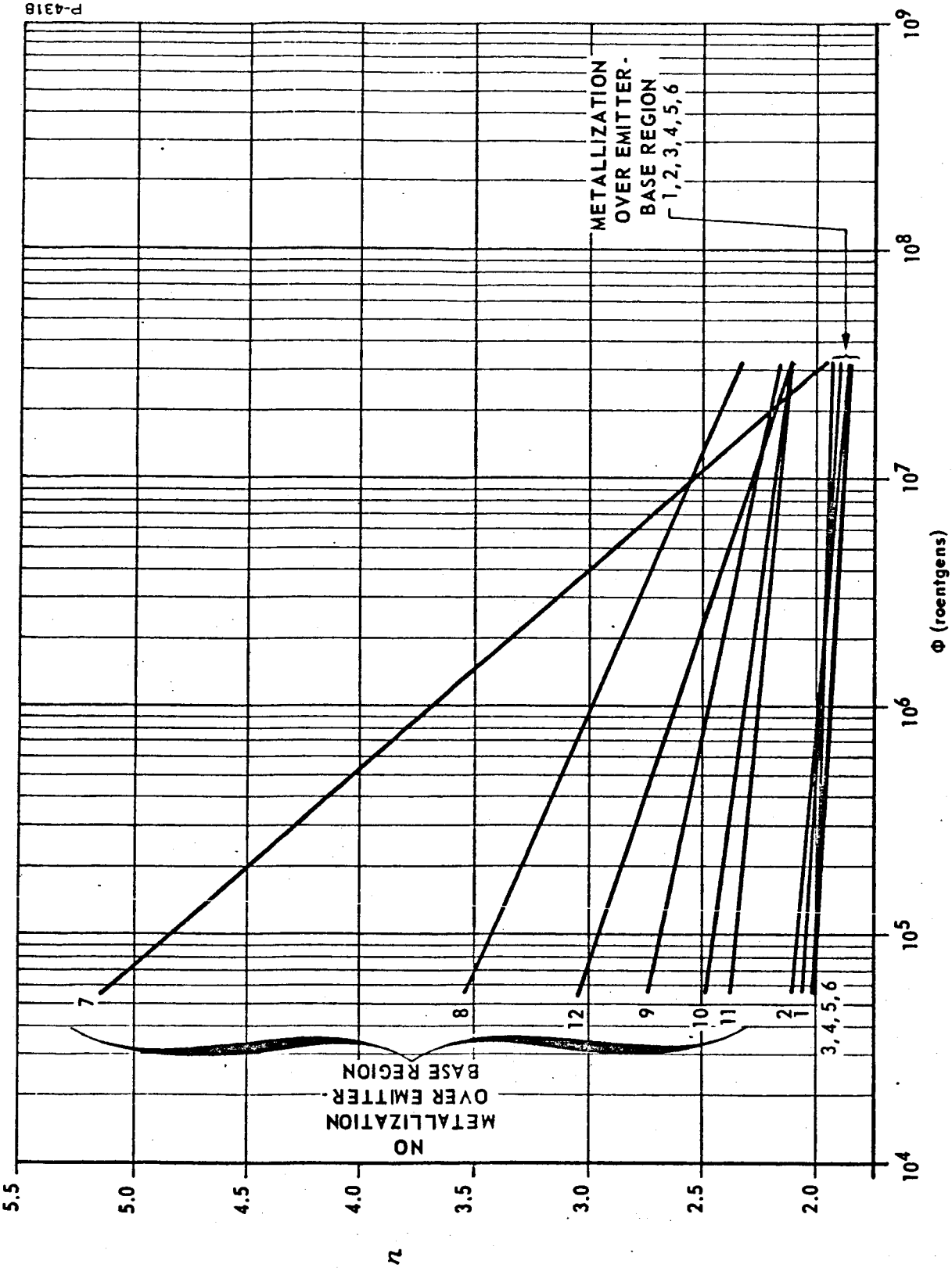


Figure 6-37 - n versus ϕ, Motorola 2N2219A

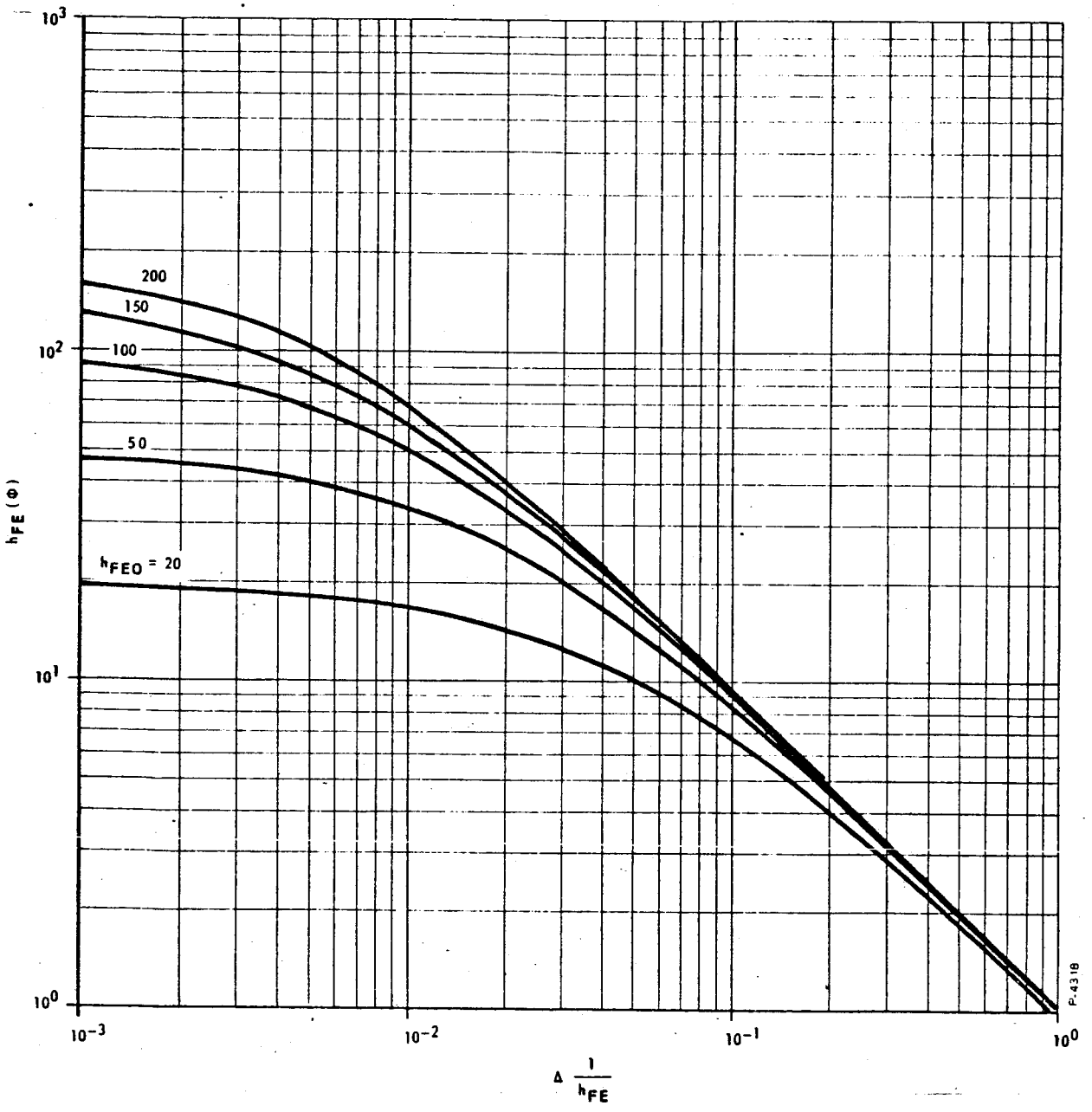


Figure 6-38 - Relationship of h_{FE} to gain degradation $\Delta\frac{1}{h_{FE}}$ for various initial h_{FE} values

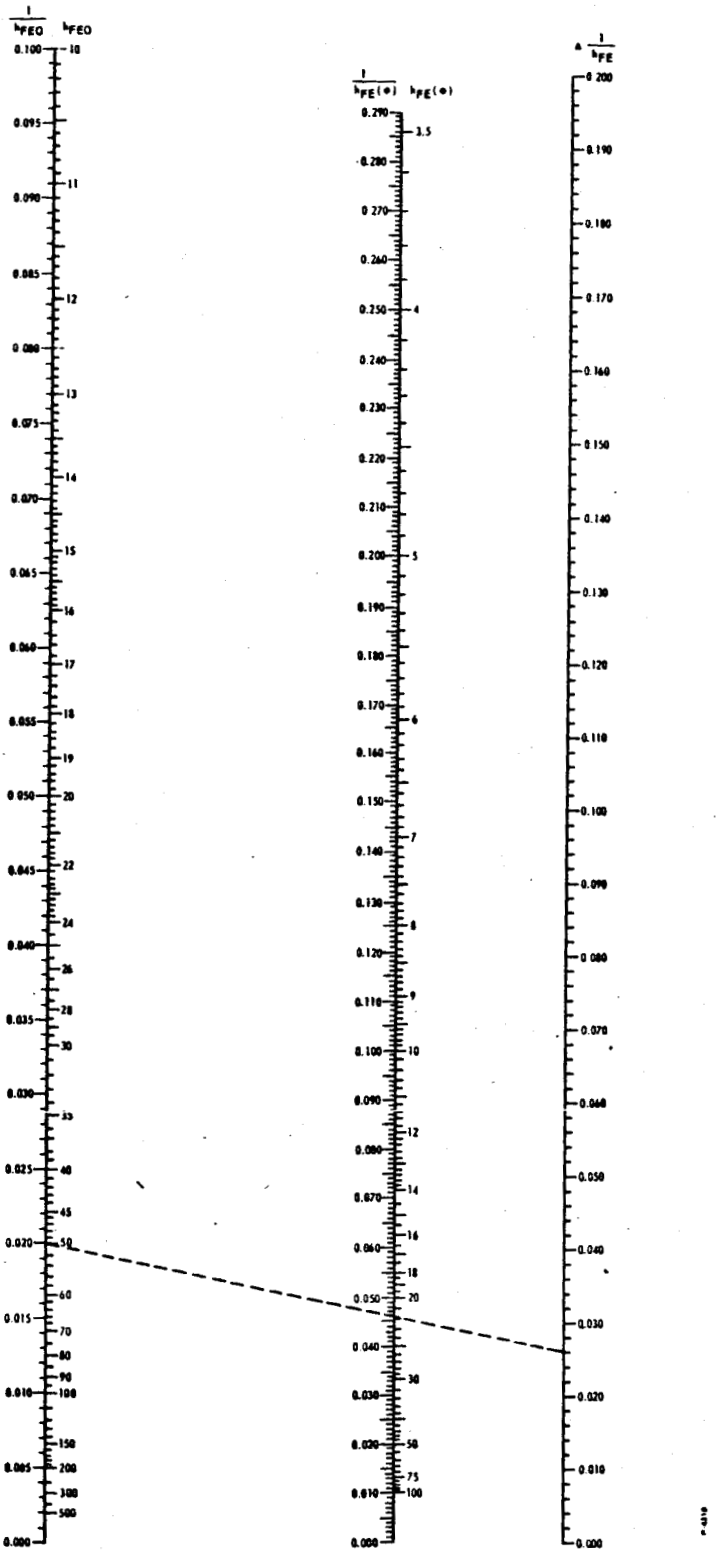


Figure 6-39 - Nomograph for relationship of h_{FE} to gain degradation $\Delta\frac{1}{h_{FE}}$

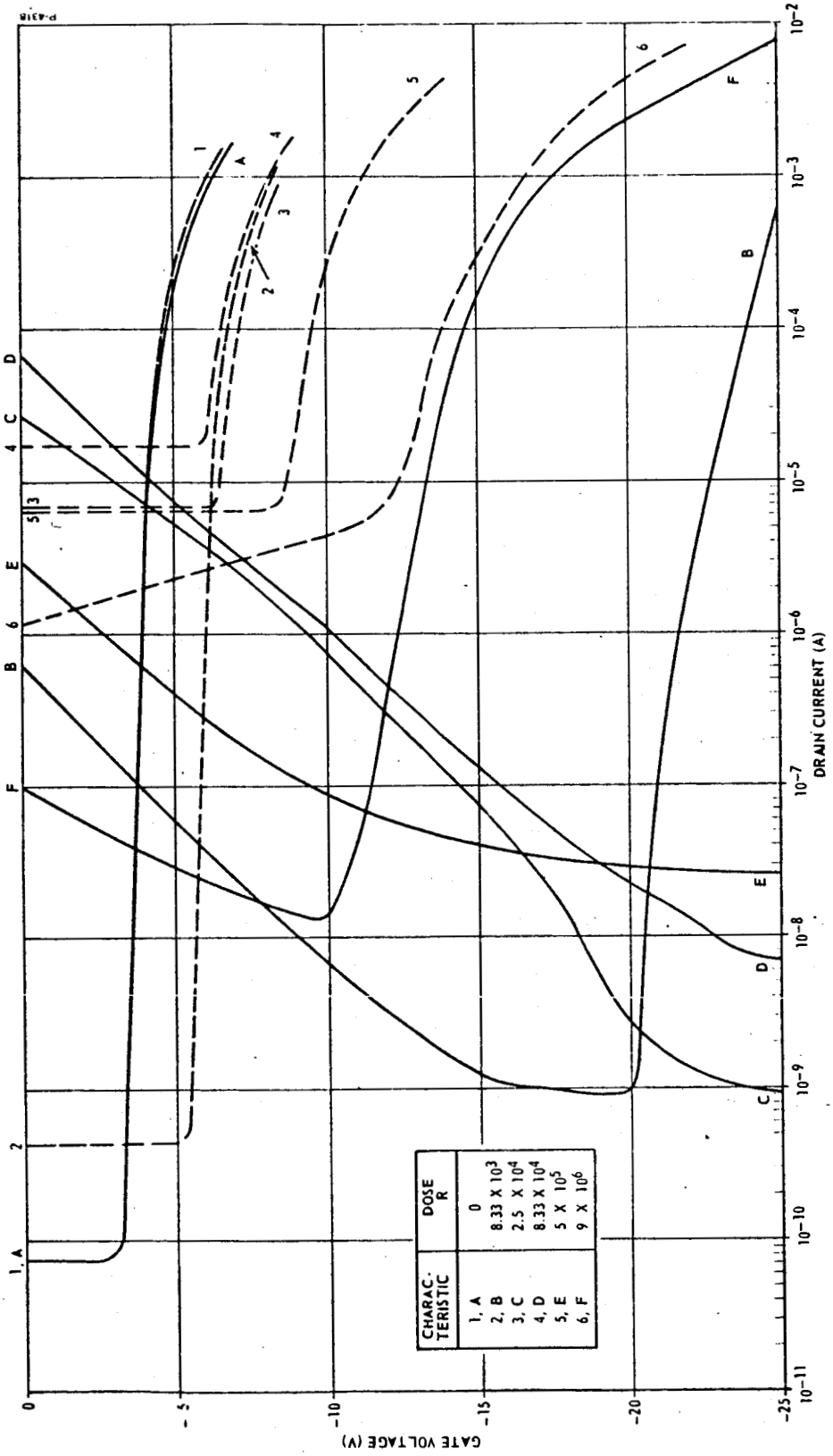


Figure 6-40 - Typical I_{DS} versus V_G characteristics as a function of dose. P-channel, MOSFET General Microelectronics 2N3609 transistor 1

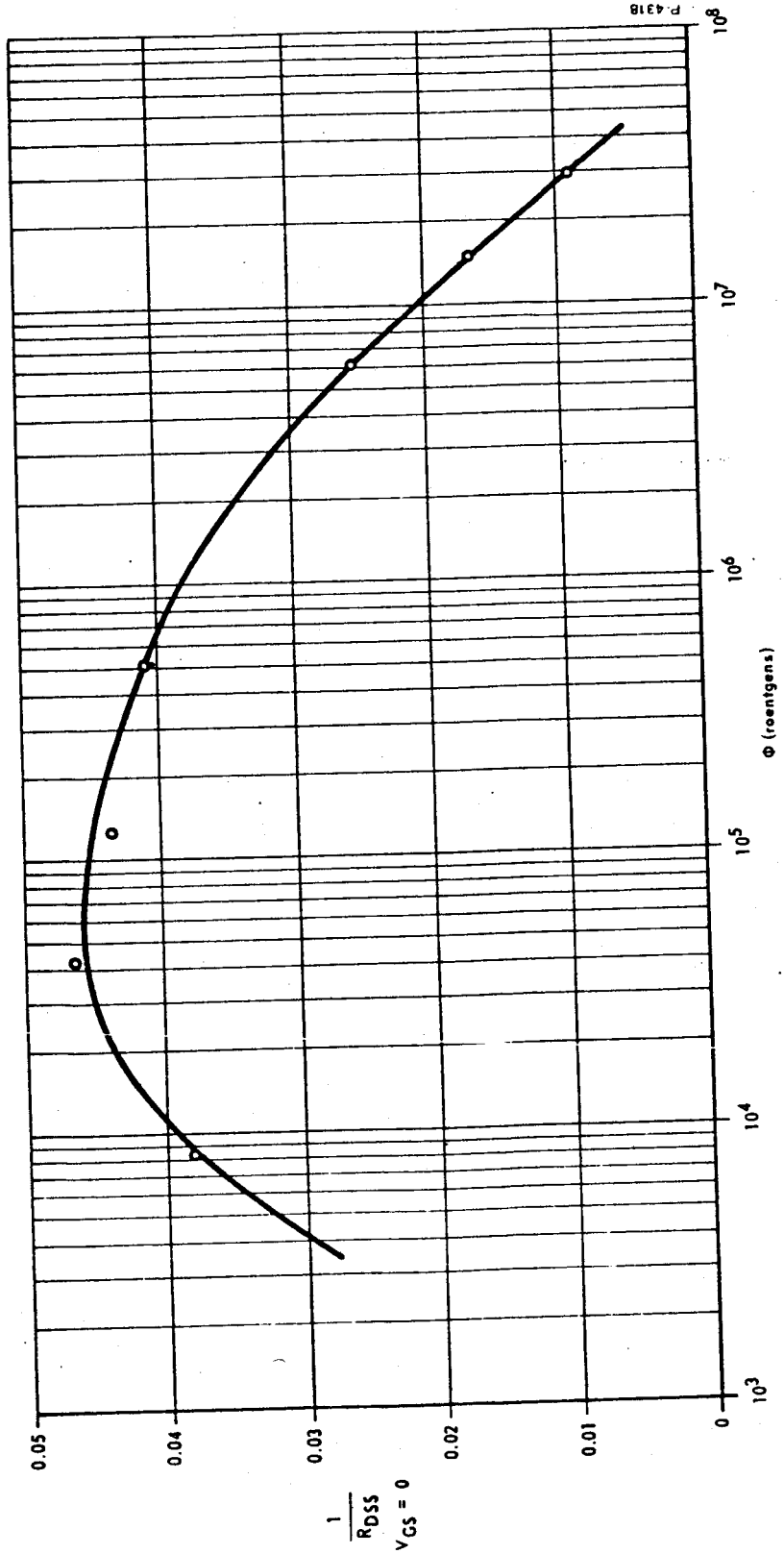


Figure 6-41 - Drain source conductance versus dose for an n-channel MOSFET (V_{GS} = +6V during irradiation)

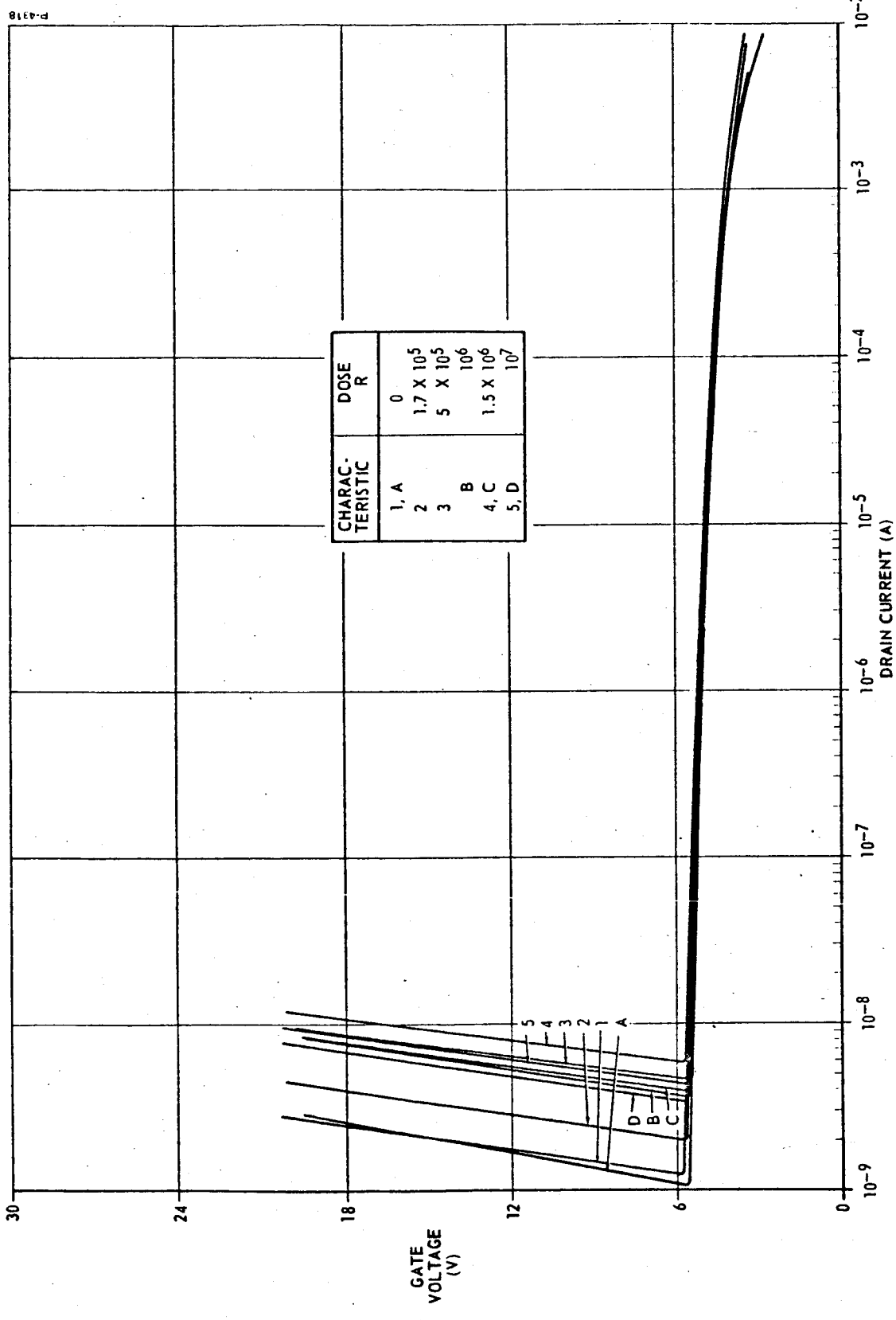


Figure 6-42 - Typical I_{DS} versus V_G characteristics as a function of dose. Junction FET, Siliconix 2N3387 transistor 7

SECTION 7

SCREENING

7.1 BASIC TECHNIQUES

The results of the device evaluation program showed that no single bipolar transistor type presently available adequately eliminates or minimizes ionizing radiation surface effects. However, since most transistor types evaluated showed a wide spread in radiation-induced surface damage, it appears that the best means of obtaining transistors with minimal susceptibility to ionizing radiation is to screen devices with poor surface properties in radiation from those with good properties. This section discusses the development of a suitable screening technique and the results of an evaluation of the technique for a variety of transistors.

There are a number of possible techniques for screening transistors with desirable surface characteristics in ionizing radiation from those with undesirable characteristics. The three considered to have the most potential were: (1) irradiation with a small dose of ionizing radiation without subsequent recovery, (2) application of an equivalent nonradiation stress, and (3) irradiation with ionizing radiation and subsequent recovery. The first technique is one in which the transistors are subjected to a small radiation dose and the amount of degradation is measured. If a reverse collector-base junction bias is used in conjunction with the radiation, the low dose data will indicate the rate at which devices are affected by the I_{CH} damage mechanism. This technique does not reveal the actual amount of h_{FE} or I_{CBO} damage nor any information concerning the I_{SRG} damage mechanism. Furthermore, although transistors tend to seek preirradiation equilibrium conditions, no attempt is made to return the transistors to these conditions; hence the device must be used in a degraded condition. A nondamaging screening technique is much more desirable, and since complete recovery of irradiated transistors was demonstrated in Phase I experiments, the technique of irradiating devices without recovery was not further considered. Simulation of the nonpermanent degradation caused by ionizing radiation was attempted by means of bias and high temperature stresses. Section 4.6 discusses attempts to correlate the damage induced by both stresses. Because this technique did not provide suitable correlation, it was unacceptable for screening.

The radiation-recovery screening technique is feasible because it is possible to recover transistors to their initial conditions and because reverse-biased collector-base junctions very effectively induce distinctive I_{CH} and I_{SRG} damage currents (See Section 4.2). This technique, which was used throughout Phase II of the program, permits irradiation of SiO_2 passivated planar transistors to doses equivalent to those the transistors will encounter in their specified environments. After the effects of the radiation have been observed, the transistors can be recovered to preirradiation conditions.

The screening test performed on 2N1613 devices consisted of irradating transistors with their collector-base junctions reverse-biased at 12V. Only three data points were needed in the screening — pre-test, after a small exposure, and after a large exposure — because the results of bias-radiation stress tests discussed in Section 4.2 indicated that the channel damage mechanism becomes dominant at small doses and that the I_{SRG} mechanism is dominant after large doses. After irradiation to about 10^7 rads, the transistors were recovered to preirradiation conditions by baking them for five hours at 300 to 320°C. This combination of bias-radiation stress and high temperature recovery constituted one cycle of the screening technique. To evaluate the screening technique and the screenability of the subject transistors, at least two screening cycles were used in each Phase II test.

Measurements were made of $1/h_{FE}$, I_{CBO}, C_{CB}, C_{EB} and reverse-biased junction V-I characteristics. The most useful data were obtained from $1/h_{FE}$ and I_{CBO} measurements. Attempts to use junction capacitance measurements for detection of channels were only partially successful. Junction capacitance for the 2N1613s increased to as high as 200 percent of original values, a radical change compared to all other planar transistors tested. The capacitance changes of most transistors could not be measured with certainty by the available impedance bridge.

Reverse-biased junction characteristics of V_{EBO} and V_{CBO}, though apparently not adversely affected either by the radiation stress or by the screening test, were of no value in device screening. In some cases V_{EBO} and V_{CBO} improved at low currents, e.g., refer to Figures 7-1,7-2, 7-3, and7-4 which show spreads of V_{EBO} and V_{CBO} characteristics for both cycles of screening. The curves of Figures 7-1 through 7-8 are typical of the radiation effects on reverse characteristics and indicate that breakdown specifications are not affected by ionizing radiation. This is apparent because the current values at the manufacturers minimum specified breakdown voltages are generally decades below the specified current at breakdown.

To observe the value of screening, consider Figure 7-9 which shows $1/h_{FE}$ degradation characteristics for one good and one poor 2N1613 transistor. Each curve is formed from data points taken from two screening cycles. The damage buildup characteristic is discussed in Section 4.2, and its shape can be seen in Figure 7-9 and in others in the report,e.g., Figure 4-2 and 4-4, to have a fast buildup at small doses and gradually saturate at higher doses. The damage characteristic for Device 40 peaks at low dose where the gain drops below 2, then saturates at a level below the peak (h_{FE} about 4) as dose increases. h_{FE} remains greater than 10 at all doses for Device 36. The differences between the surface behavior of the two devices is even more striking on the semilog plot of Figure 7-10.

Since the shape of the damage characteristic of the 2N1613 was well known, data were recorded at only one low dose point near the peak to insure that sufficient charage was induced in the surface to effect channels, and at one data point after a large dose ($\phi \doteq 10^7$R). This technique

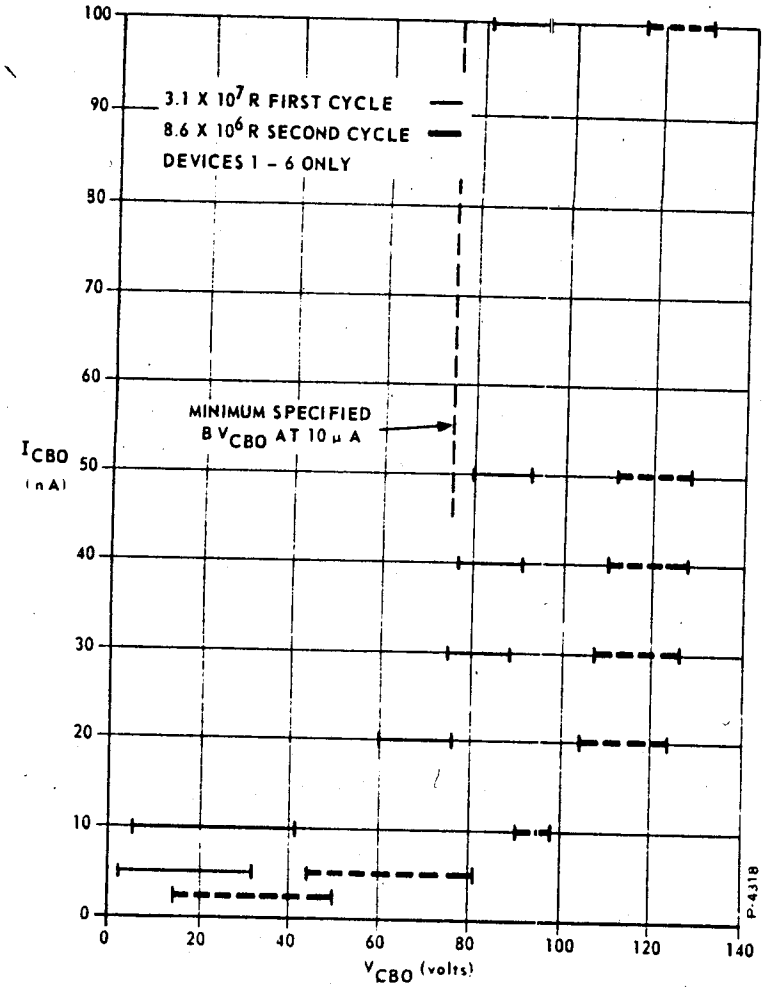


Figure 7-1 - Spread of reverse V_{CBO} characteristics after large dose, Motorola modified 2N2219A

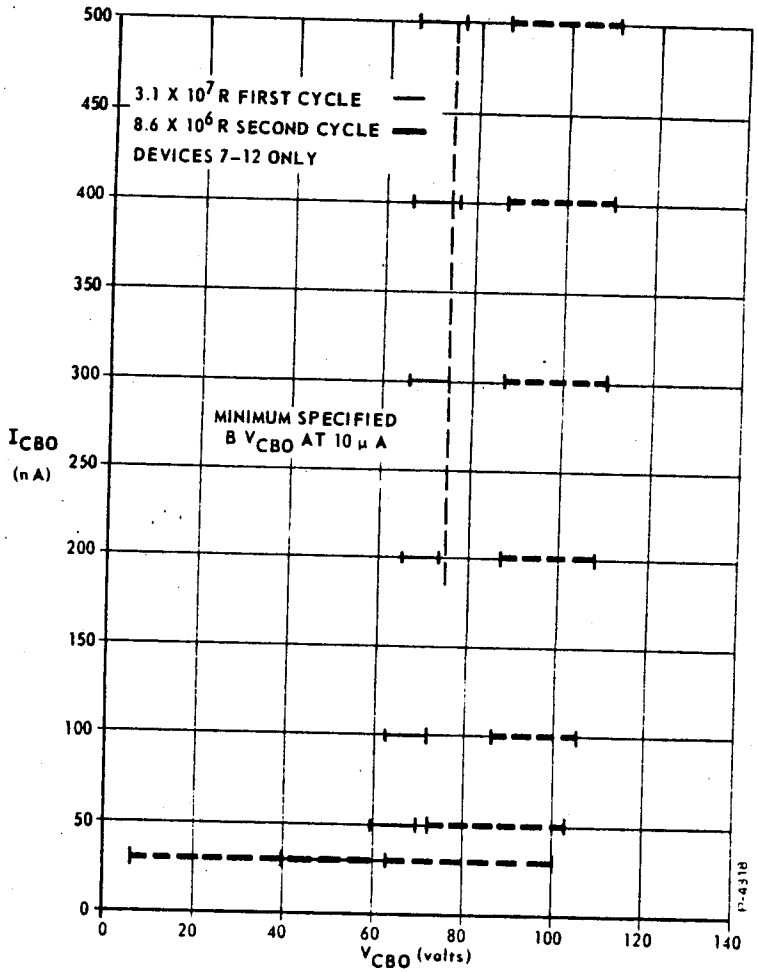


Figure 7-2 - Spread of reverse V_{CBO} characteristics after large dose, Motorola 2N2219A

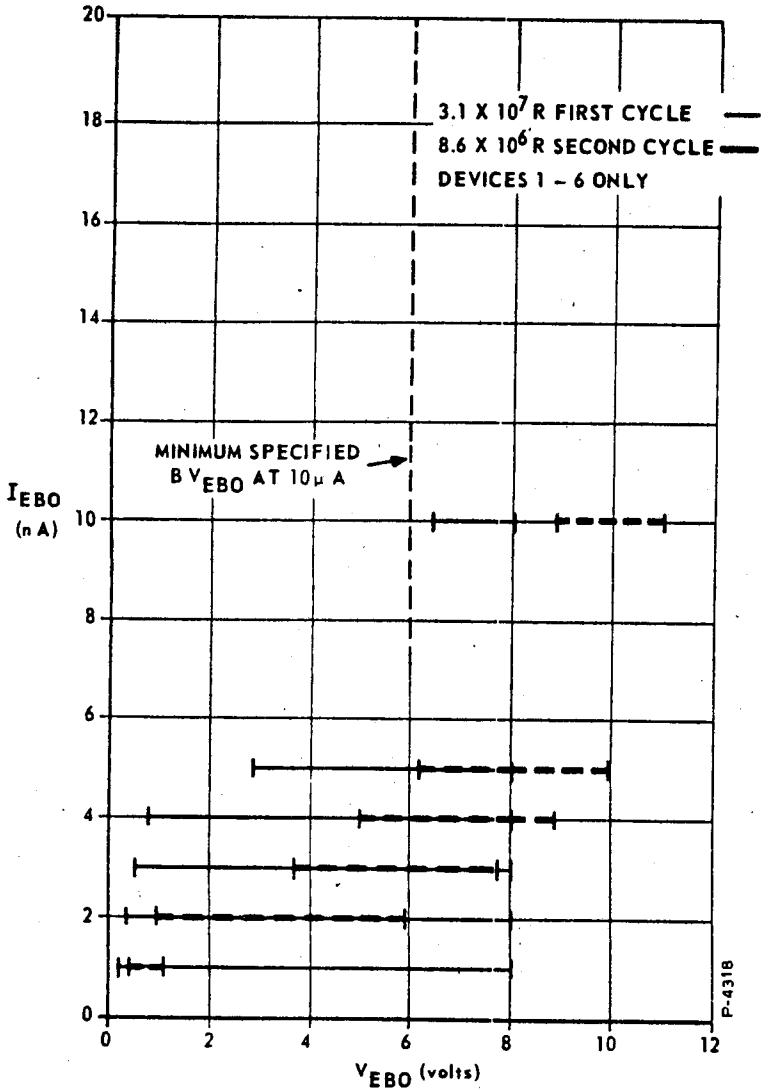


Figure 7-3 - Spread of reverse V_{EBO} characteristics after large dose, Motorola modified 2N2219A

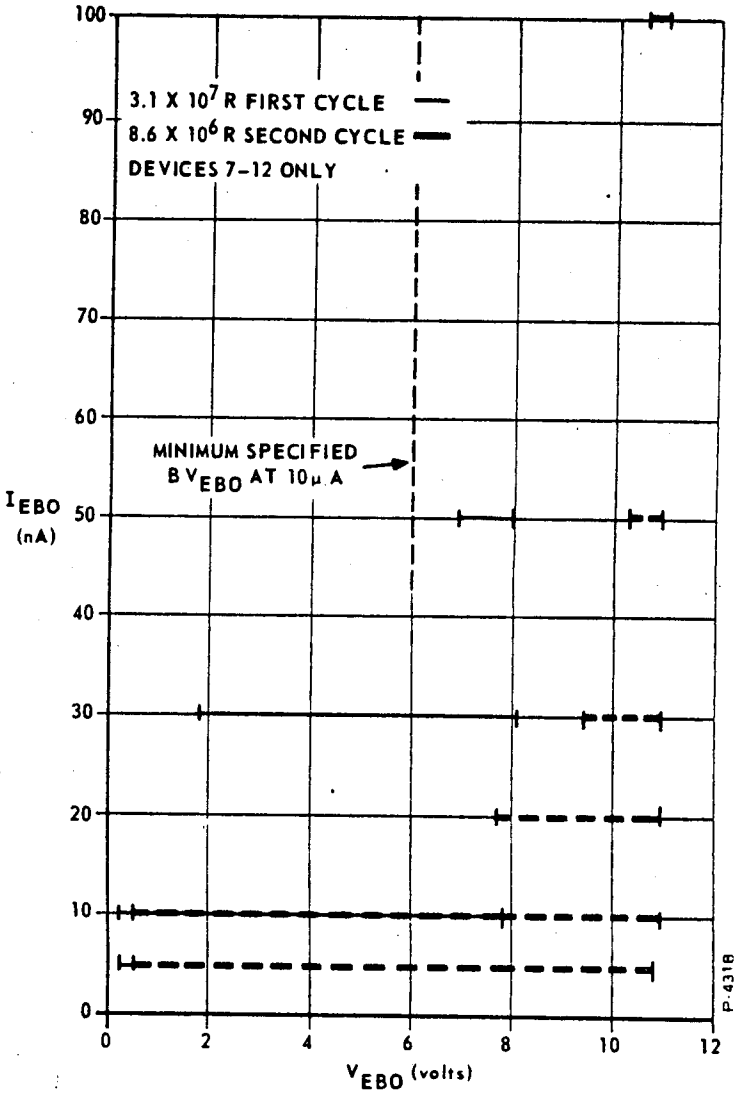


Figure 7-4 - Spread of reverse V_{EBO} characteristics after large dose, Motorola 2N2219A

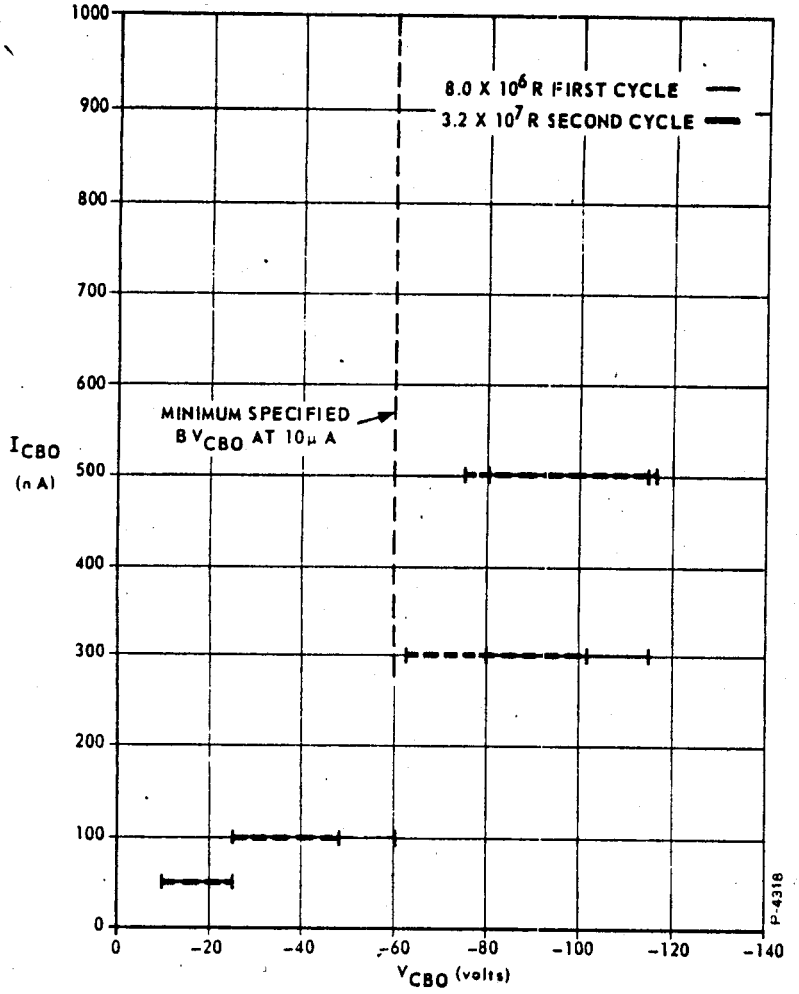


Figure 7-5 - Spread of reverse V_{CBO} characteristics after large dose, Motorola 2N2905

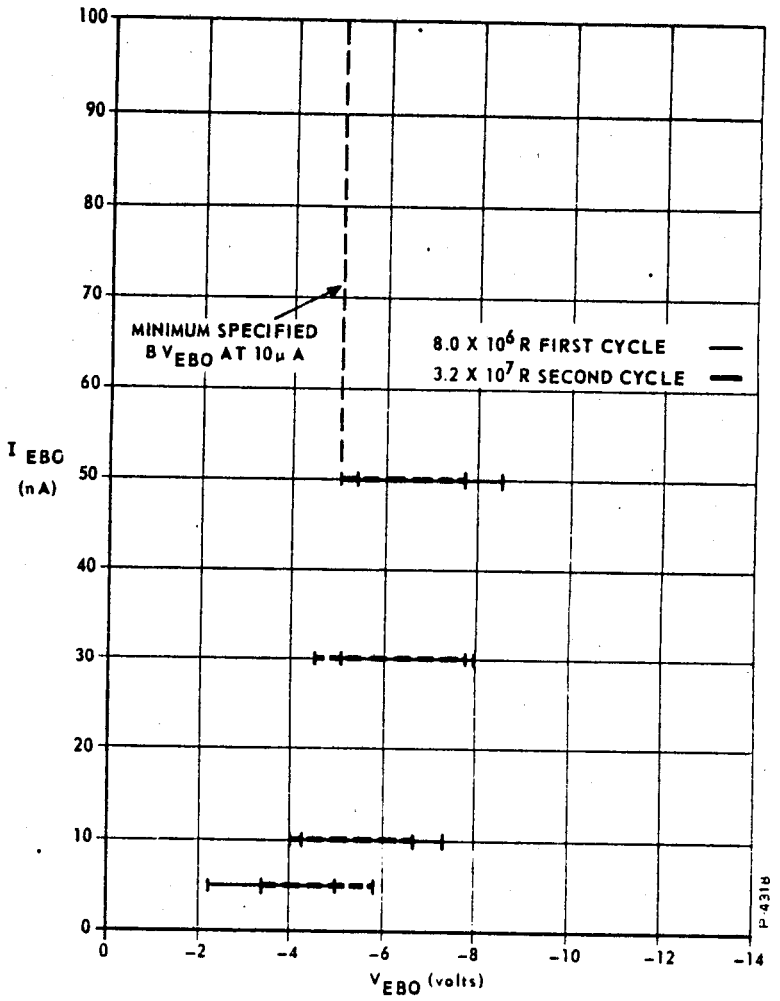


Figure 7-6 - Spread of reverse V_{EBO} characteristics after large dose, Motorola 2N2905

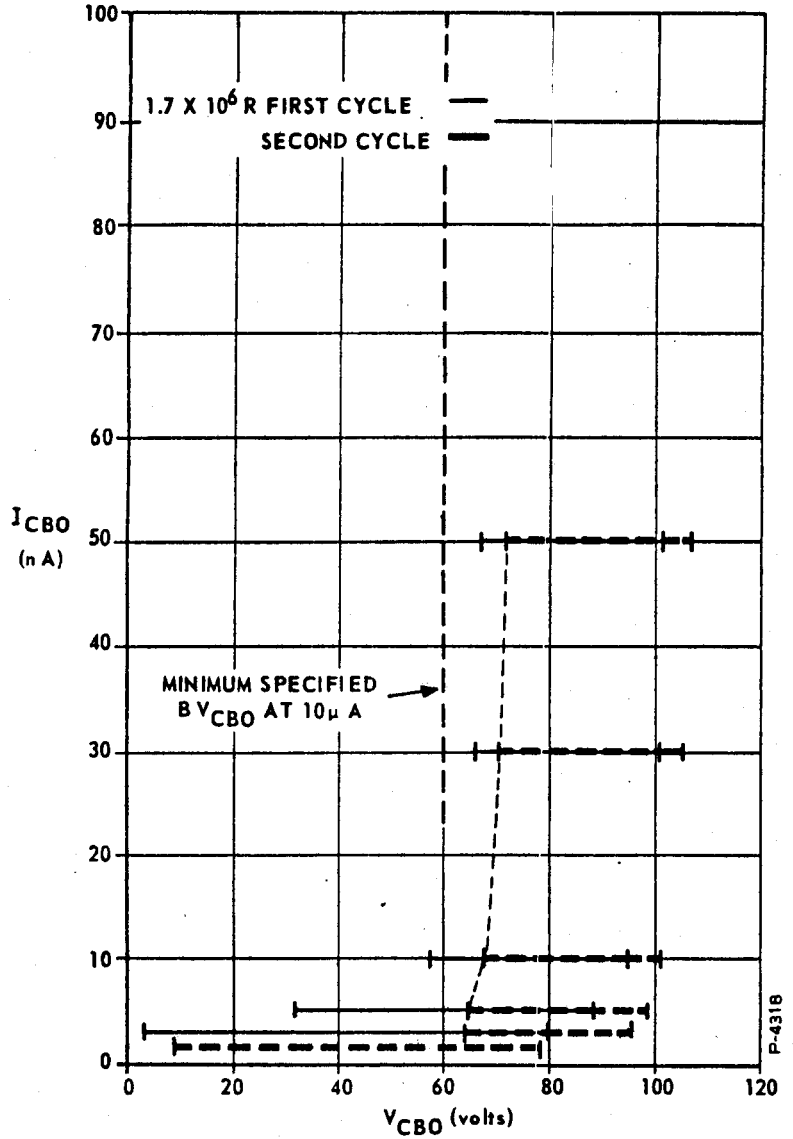


Figure 7-7 - Spread of reverse V_{CBO} characteristics after large dose, Fairchild 2N2222

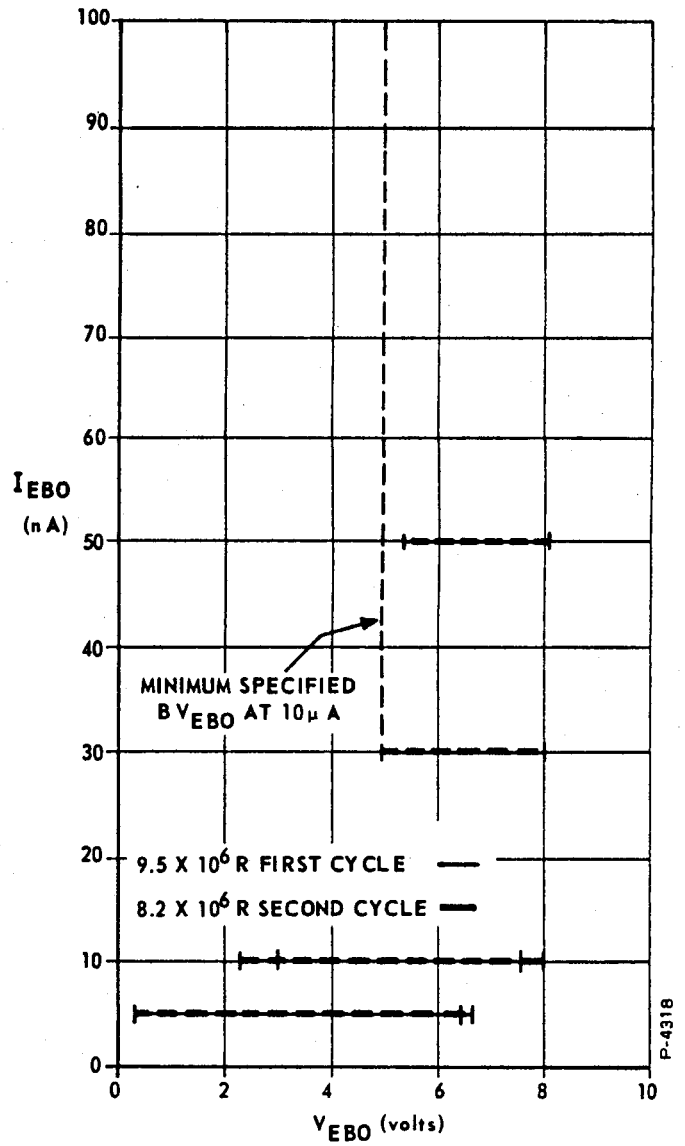


Figure 7-8 - Spread of reverse V_{EBO} characteristics after large dose, Fairchild 2N2222

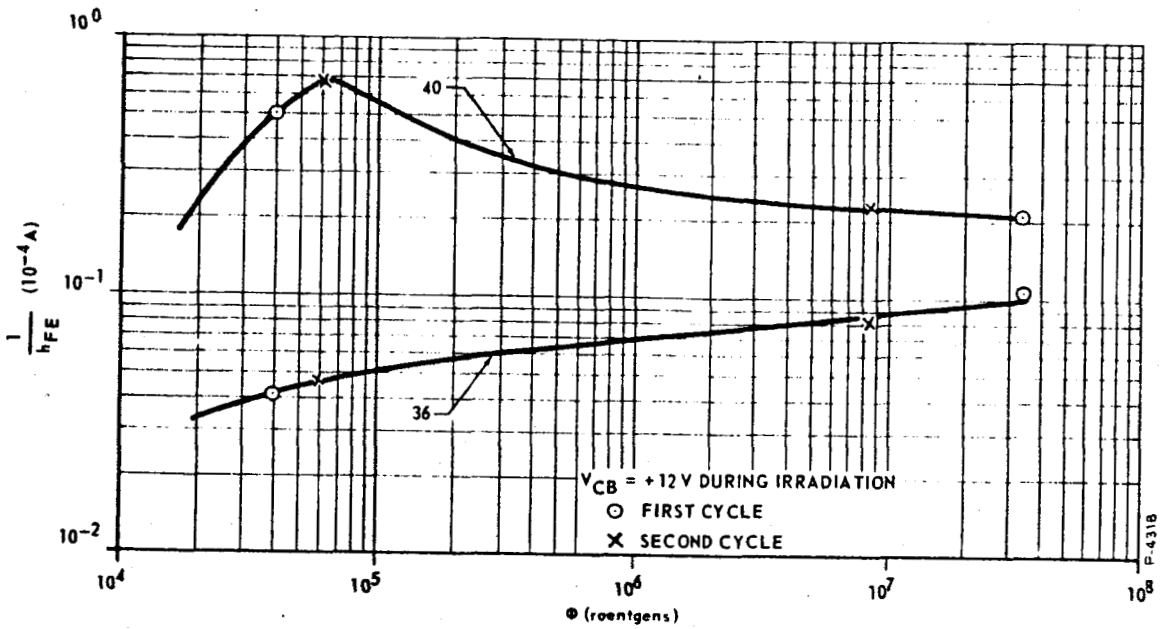


Figure 7-9 - Log log plot $1/h_{FE}$ versus ϕ for two cycles of the screening test, 2N1613 transistors 36 and 40

for evaluating screening was applied to all bipolar transistors tested in Phase II. Screening of an unfamiliar transistor type necessitates more complete testing with many low dose data points on a few test subjects. In the Phase II tests, capacitance measurements were made on a few test transistors at various doses to monitor the formation of a channel and to determine when it reached the peak. When the damage buildup characteristics are known, fewer points are needed in the actual screening cycle.

7.2 EVALUATION OF THE SCREENING TECHNIQUE

7.2.1 Basis for the Evaluation

The screening technique was evaluated for its ability to provide three kinds of information: (1) the magnitude of the induced h_{FE} and I_{CBO} degradation for any device type, (2) the spread of induced damage among a number of samples of a type, and (3) the repeatibility of damage with dose after a device has been irradiated and the damage removed. The latter two were given major emphasis in the evaluation. Eliminating devices which show abnormal surface behavior under irradiation in comparison with the others in a sample, reduces the spread, thus facilitating prediction of the magnitude of damage, because of the greatly improved repeatability, in subsequent cycles of irradiation. In addition, the reliability of the remaining samples should be improved since the abnormal devices have poor quality interfaces, which generally means poor reliability. This topic is discussed more fully in Section 7.2.3.

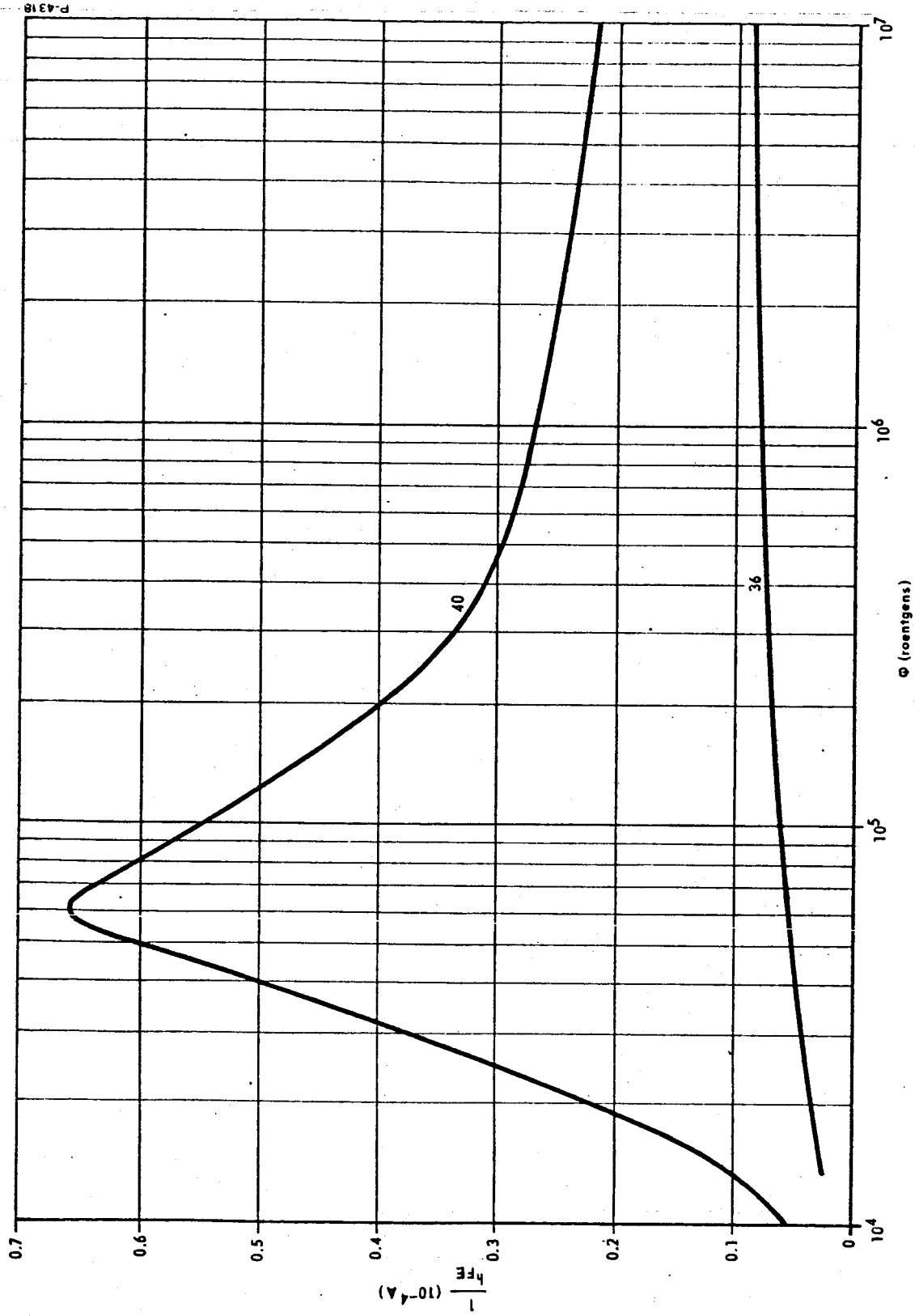


Figure 7-10 - Semilog plot of damage for 2N1613 transistor 36 with good surface characteristics and 40 with poor surface characteristics

Once the spread in damage is minimized by screening the magnitude of the damage for a subsequent irradiation is reasonably predictable and the application will dictate whether the device type with its predicted changes is acceptable for the intended circuit. For this reason, the first utilization of screening is to reduce the spread in damage among devices of a type by eliminating those with abnormal surface behavior. The second utilization is to eliminate types of transistors which have gain and leakage current changes with radiation that are prohibitive at the desired operating current for a particular circuit.

Data used in the evaluation of the screening techniques are depicted in the plots of Figures 6-1 through 6-32 in Section 6. Figures 6-1 to 6-12 are plots of two cycles of the 12 Phase II screening tests, showing graphically two points of $1/h_{FE}$ and I_{CBO} as a function of dose for each cycle. Damage was removed by means of the standard recovery technique prior to the second irradiation. Because the dose is shown logarithmically, the initial values of $1/h_{FE}$ and I_{CBO} prior to each cycle are given in tables on each graph. Figures 6-13 to 6-32 show the spreads in $\Delta \frac{1}{h_{FE}}$ due to radiation as a function of the measurement current for all bipolar transistors tested. The plots depict the data obtained at the low dose level ($\sim 10^4$R) and high dose level ($\sim 10^7$R).

The initial value tables on each of Figures 6-1 to 6-12 reveal that planar SiO_2 passivated transistors recovered to nearly pre-irradiation h_{FE} and I_{CBO} values. In fact, many transistors recovered to better than their original conditions. Repeatability cannot be evaluated accurately on the basis of a single point at low dose, however, because the high rate of h_{FE} and I_{CBO} degradation buildup at small doses makes it difficult to achieve a data point at equivalent damage levels after reirradiation.

The two-point-per-cycle screening of several transistors does not show the peak values of h_{FE} and/or I_{CBO} degradation for all transistors because each transistor peaks at a somewhat different dose. The utility of this method of screening is in separating devices with relatively poor surface interfaces from those with good interfaces.

7.2.2 Screening for Radiation Tolerance

The procedure for screening was to eliminate those transistors whose electrical parameters degraded more significantly than others of the same type when subjected to the same ionizing radiation stress. No attempt was made to assign an acceptable numerical value to either the amount of I_{CBO} or $1/h_{FE}$. Transistors which departed from the group in h_{FE} and I_{CBO} damage or whose slope constant n indicated poor interface regions were disqualified. Results of screening based on eliminating transistors with poor interface regions from Figures 6-1 through 6-12 (cycle 1 data) are shown in Table 7.1. Devices screened out and the reasons for their elimination are presented, as well as data showing improvements in gain and leakage current due to screening. Data prior to screening pertain to Cycle 1, and data after screening pertain to Cycle II.

Table 7-1 - Transistors screened out as a result of Phase II screening tests

Transistor Type	Devices Screened Out	Reason	Min* h_{FE} Prior to Screening at 10^{-4}A	Min* h_{FE} After Screening at 10^{-4}A	Max* I_{CBO} Prior to Screening (nA)	Max* I_{CBO} Prior to Screening (nA)
2N1613	40, 45 44	h_{FE} low at early dose I_{CBO} high	2	8.3	141	10
2N2222 (Mota)	1, 2, 3, 4, 9 6, 7	h_{FE} low, two noticeable groupings I_{CBO} high, second cycle	3.4	14.3	17.5	0.65
2N2219 (Mota)	7 7	h_{FE} low I_{CBO} based on two cycles	1.25	6.25	7.5	1.1
2N2905 (Mota)	None	Transistors improved by screening test	3.1	11.1	20	27
2N2222 (FSD)	None	Responses grouped closely, first cycle	5	3.85	2.7	2.3
2N1132	2, 5, 11, 12 8	h_{FE} low, first cycle h_{FE} low, second cycle	1.25	11.1	30	15
2N722 (TI) (Mota)	7, 8, 9, 10, 11, 12	h_{FE} low, two noticeable groupings	2.63	10.9	20	20
2N3058	2, 3, 4, 6	I_{CBO} high	7.15	17.25	1270	2.5
2N3964	10 8, 9	h_{FE} low, first cycle h_{FE} low, second cycle	7.1	15.6	3.7	1.5
TD106	7, 8, 11 3	h_{FE} low I_{CBO} high	5.7	13.3	945	92

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*h_{FE} and I_{CBO} data given for small doses; $10^4 \leq \phi \leq 10^5$ R.

The improvements gained by screening are displayed in the reduction in the spreads of $\Delta\frac{1}{h_{FE}}$ versus I_C characteristics in Figures 6-13 through 6-32. Screening out the devices listed in Table 7-1 reduced the total $\Delta\frac{1}{h_{FE}}$ spreads to the broken-line curves that appear with the spreads in many of the figures. The upper and lower $\Delta\frac{1}{h_{FE}}$ values after screening are listed in Table 7-2 for the same two current levels used to show the spreads of nonscreened transistors in Table 6-2. The improvements in the spreads of $\Delta\frac{1}{h_{FE}}$ due to screening are readily seen by comparing the upper and lower values for each device type in Tables 6-2 and 7-2.

At low currents -- two, three or more decades below the nominal (peak h_{FE}) operating current -- the improvements due to screening are quite pronounced, particularly at low doses. Overall reliability at low doses is also expected to be improved by this screening. At higher doses or higher currents, the spread in damage is not as great, therefore screening serves only to confirm this fact and indicate the magnitude of damage that can be expected.

7.2.3 Screening for Reliability

Ionizing radiation screening is not only beneficial for investigating the radiation tolerance of transistors but is also an excellent means of determining the quality of the surface $Si-SiO_2$ interface region which many investigators believe to have a major influence on the reliability of transistors. If the surface interface quality is poor, nonradiation environments can subject transistors to stresses which will cause charge buildup in the oxide and electrical parameter degradation similar to ionizing radiation. As an illustration, Figures 4-5 and 4-6 indicate that the interface region of Device 8 is much poorer than Device 15 by the pronounced dominance of the channel mechanism and higher leakage current levels-about two orders of magnitude. Elimination of devices with characteristics similar to those of Device 8 from use in nonradiation as well as radiation environments should enhance system reliability significantly, although this assertion has not been proved explicitly in this program since it was not included in the scope of work.

7.3 APPLICATIONS OF SCREENING

Screening can be performed either by the user of semiconductor components or by the manufacturer of semiconductor devices. It is applied to lot acceptance tests by satistical sampling and/or as a means for determining the best of a number of devices to use for radiation environments. The manufacturer could screen a much larger number of units than the user, probably before transistors are encapsulated. Therefore the type of equipment and the procedures may differ somewhat between the manufacturer and the user.

Table 7-2 - Spreads of $\Delta\frac{1}{h_{FE}}$ after screening

Transistor	Current used for Evaluation (A)	Spread of $\Delta\frac{1}{h_{FE}}$ after screening (data x 10^{-3})			
		Small Dose		Large Dose	
		min	max	min	max
2N1613	10^{-4}	26	75	90	180 (1)
	10^{-2}	3	5	12	18 (1)
2N2222 (Mota)	10^{-4}	21	58	42	160 (1)
	10^{-2}	2	3	4	18 (1)
2N2222 (FSD)	10^{-4}	40	70	50	120 (1)
	10^{-2}	3.3	6	5	12 (1)
2N2905	10^{-3}	24	84 (2)	130	240 (2)
	10^{-1}	3	7 (2)	1.6	1.8 (2)
2N1132	10^{-4}	18	68	95	440 (1)
	10^{-2}	2.6	4.6	10	27 (1)
2N722 (TI)	10^{-4}	40	76 (2)	157	240 (2)
	10^{-2}	6	8.5 (2)	13	18 (2)
2N722 (Mota)	10^{-4}	160	350 (2)	270	1000 (2)
	10^{-2}	16	28 (2)	30	55 (2)
2N3058	10^{-4}	40	100 (2)	65	160 (2)
	10^{-2}	15	30 (2)	20	47 (2)
2N3964	10^{-4}	50	85	560	760 (1)
	10^{-2}	4.2	7	31	40 (1)
2N2219A (Metallized)	2×10^{-4}	54	65 (2)	90	100 (2)
	2×10^{-2}	5.1	6.3 (2)	11.8	13 (2)
2N2219A (Nonmetallized)	2×10^{-4}	50	73	110	125
	2×10^{-2}	3.3	3.7	12.5	13.5
TD106 (Metallized)	10^{-5}	21	40 (2)	140	160 (2)
	10^{-3}	3.3	6.2 (2)	18	20 (2)
TD106 (Nonmetallized)	10^{-5}	68	250	180	490
	10^{-3}	6.8	12	13.5	23

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(1) Screening has no effect at large dose.

(2) No transistors screened out.

The basic procedure for screening is to irradiate the reverse-biased transistors with a suitable ionizing radiation source to a moderately low radiation dose. The optimum level of radiation for screening varies with the device type and should be determined by appropriate experiments prior to establishing the screening cycle. n-p-n transistors should be irradiated to the approximate level at which the damage peaks in most devices. p-n-p transistors should be screened near the levels they are expected to receive in the final application. (Results of the experiments performed in this program indicate that the optimum dose for screening is between 10^4 and 10^5R.) Measurements are made to ascertain leakage current changes and gain changes at moderately low current levels. After eliminating those devices for which the sample irradiated shows changes in excess of the norm, the remaining devices are returned to their original condition (or better) by a 3- to 5-hour bake at 320°C.

As an example of the capability of typical laboratory equipment for performing this task, the Siefert X-ray facility used in this program will accommodate 40 transistors at a radius of one inch from the source. An irradiation period of about 20 minutes will provide the required dose at a rate of 100R/s at this radius. Larger sample sizes can be accommodated by increasing the radius, but the resultant lower dose rates require larger exposure times which rapidly become prohibitive. As a result, the product of exposure time and sample size is not better than 1000 unit-days. The approximate cost for a screening facility of this type is $15,000.

Because the manufacturer could screen transistors prior to encapsulation, he could use an electron source of ionizing radiation capable of a much higher dose rate. Dose rates of 10^4R/s are easily achieved for areas of 100 in^2, thus 100,000 or more devices (360 slices of 300 devices/slice) could be irradiated to 10^5R in 10 seconds. With this technique, devices that fail to meet ionizing radiation tolerance specifications can be eliminated by the manufacturer prior to packaging. The screening test requires that each device be probed to measure acceptable parameters, but industry commonly uses this practice in testing for other parameter specifications. The estimated cost of such a facility is on the order of $50,000, but the ultimate cost to the user per transistor would be small because of the large numbers tested and short irradiation times required. Furthermore, such a facility could be easily incorporated into a manufacturer's processing and fabrication facility.

SECTION 8

CONCLUSIONS AND RECOMMENDATIONS

8.1 CONCLUSIONS

Ionizing radiation produces three mechanisms of damage in silicon planar transistors attributable to the alteration of surface properties. These damage mechanisms cause degradation of h_{FE} and I_{CBO} as demonstrated by experiments with X-rays with energies below that necessary to produce bulk effects, but sufficient to induce surface charge. The induced charge can migrate in the SiO_2 under the influence of electrical bias fields and cause the growth of channels which have varying effects on the electrical parameters, depending on the quality of the Si-SiO_2 interface and the operating current. The variables that influence ionizing radiation surface damage include, in addition to the radiation dose, the electrical bias applied to the emitter-base and collector-base junctions during irradiation, the measurement current (or current at which the damage is evaluated), the ambient environment surrounding the transistor chip, the purity of the Si-SiO_2 interface, the transistor material (n-p-n or p-n-p), and any special surface treatments (field plate, guard ring, etc.).

Two of the three mechanisms of damage are effective at low operating currents, where they produce additional base current components. One is a channel current I_{CH}, and the other is an increase in space charge recombination-generation current I_{SRG}; both reduce low current h_{FE} and increase I_{CBO}. The third mechanism increases base region surface recombinations, thereby degrading h_{FE} at high current levels where emitter crowding forces a greater fraction of the emitter current to the surface region.

Degradation of h_{FE} induced by I_{SRG} and I_{CH} is identifiable by exponential slope constants n, where n for I_{SRG} is between 1.5 and 2, and for I_{CH} is greater than 2. This identification method does not quantitatively identify the two components but instead indicates which of the two currents is dominant. Junction capacitance measurements also are used for monitoring the formation and decay of channels in some devices.

Surface damage for n-p-n transistors is characterized by a rapid rise in $1/h_{FE}$ or I_{CBO} at low radiation doses due to the formation of a channel. At higher doses the channel recedes due to photoemission of electrons, and the damage levels off to a saturation value. For p-n-p transistors, damage buildup with dose is more gradual, but the channel does not recede and the damage continues to increase with dose. In general, the damage induced at low doses ($< 10^4$ rads) tends to be smaller in p-n-p transistors than n-p-n transistors and vice versa at higher doses ($> 10^5$ rads). However, this comparison cannot be made categorically since there are wide variations within each group of devices.

The amount and rate of buildup of h_{FE} and I_{CBO} degradation produced by ionizing radiation dose are dependent on electrical bias during irradiation. Both the magnitude and rate of degradation with dose are most severe for reverse-biased junctions where the channel component of current dominates the behavior. Zero-biased and particularly forward-biased junctions have a lower rate of damage buildup with dose and a lower damage level at saturation since I_{SRG} dominates rather than I_{CH}.

The effect of the gas ambient (usually nitrogen) surrounding the transistor chip is to promote channel formation and the I_{CH} component of current when transistors are reverse-biased during irradiation. Devices evacuated and reverse-biased during radiation had considerably less damage at low doses ($< 10^5$ rads) than those with a nitrogen ambient; but at high doses ($> 10^5$ rads) there were no differences between evacuated and nonevacuated devices. Similarly, no significant difference was observed between normal nitrogen ambient and a vacuum for devices with passive or forward biases during irradiation. Vacuum therefore is effective in reducing damage at low to moderate doses in reverse-biased (cutoff) transistors.

The model proposed to explain the behavior of bipolar planar transistors in ionizing radiation is consistent not only with the results of this experimental program but also with the results of others studying the effects of ionizing radiation on MOS structures.

Evaluation of a variety of transistor types — off-the-shelf as well as experimental with special surface treatments — from a variety of manufacturers, revealed that for bipolar transistors, no single type, manufacturer, or process offered immunity to ionizing radiation. In most cases, variations of surface effects within a given type of device were greater than the variations among many different types and manufacturers. The devices with special surface processes generally showed a smaller spread of damage in any one device type and greater repeatability than the standard device possibly due to a tighter process control during their manufacture. However, exceptions to this rule as well as the limited effort provided in the program prevent consideration of the special process as a complete solution. The process that consistently resulted in improved behavior in ionizing radiation was the metallization over the emitter-base junction. This metallization impedes emitter-base junction channeling and therefore reduces h_{FE} degradation at low doses. It does not reduce the damage as significantly at high doses or high currents, however.

The annular or guard ring process appears to provide no tolerance to radiation-induced damage for n-p-n devices. All p-n-p devices tested had a band-guard structure thereby preventing any evaluation of the improvement due to that structure. However, Stanley reported large improvements in I_{CBO} sensitivity due to a band guard.[5.8] Tri Rel and Planar II processes have little effect on h_{FE} degradation but do reduce I_{CBO} variations with radiation, and the damage among devices of a type has a smaller spread.

Of all the devices evaluated on this program, the most radiation-tolerant with respect to change in gain characteristics as a function of

dose was the p-channel junction field effect transistor. The example used in the program was the Siliconix 2N3587. Although gate leakage with radiation did increase, thereby causing a reduction in input impedance, the changes were so small that they would affect only circuits requiring extremely high input impedances. Of all the devices evaluated, MOSFETs were the most severely affected by ionizing radiation. Their use in radiation environments should be restricted to low doses ($< 10^3$R) and linear circuits.

In this program no preradiation measurements of device electrical parameters were found to correlate with surface damage effects to provide a nonradiation technique for predicting transistor tolerance to ionizing radiation. The X-ray high temperature screening cycle shows promise as a prediction technique since it eliminates transistors with poor surface properties from the test subjects, leaving those with more predictable surface characteristics. However, further experiments are required in order to establish effective screening cycles. An additional result of this program is that metallization over the emitter-base region was shown to be effective in reducing h_{FE} degradation in ionizing radiation for two types of n-p-n devices.

8.2 RECOMMENDATIONS

Two areas are shown by the results of this program to have a good potentiality for leading to the minimizing of surface effects of radiation. These areas are bias-radiation screening and base-emitter metallization. Additional studies in these areas are strongly recommended. Further studies are also recommended of radiation rate effects and temperature effects.

Further studies of screening are needed to optimize the screening procedure and to determine the effects of screening on reliability (improvements as well as drawbacks). Screening procedures vary with respect to who performs them. When performed by the manufacturer, the procedures must be compatible with large-scale, rapid production processes. An individual user can perform screening with a smaller, less complex installation. The variables that need to be studied experimentally include: radiation rate, electrical bias, number of data points, radiation dose, measurement conditions, measured parameters, temperature and time for recovery, ambient conditions (e.g., screening in vacuum may lead to improved surface stability), and limitations of screenable devices.

The effects of screening on device reliability need to be examined, focusing on two aspects: (1) the possible improvements in the overall reliability of a batch of transistors after all those with poor surface stability or $Si-SiO_2$ interface have been screened out, and (2) the degradation in reliability of the remaining transistors after subjection to high-temperature recovery.

Base-emitter metallization effectively reduced the surface sensitivity to radiation of two experimental devices evaluated in this program at low currents and small doses (e.g., reduced or eliminated base-emitter channeling). Additional studies and experiments are needed to determine the effectiveness and limitations of metallization for transistors other than the two types tested.

Understanding the two areas of rate effects and temperature effects is important not only because of their effect on screening but also to complete the technological understanding of surface radiation effects.

The rate experiments performed in this program resulted in a multiplicity of mechanisms occurring simultaneously, thereby preventing interpretation of results. Additional rate experiments with appropriate bias conditions would enable separation of the mechanisms by procedures similar to those used previously in this program. Dose rate data are important due to the wide range of ionizing radiation rates generated by space environments, propulsion and power reactors, and nuclear weapons. An accelerator as well as an X-ray machine would be used for studying rate effects.

Actual radiation environments in which devices would be used encompass a wide operating temperature range (-55°C to +150°C is not unusual). All test data thus far on ionizing radiation effects were taken at room temperature. Expanding the understanding of surface effects over the expected operating temperature range will enable the electronics designer to design for a realistic environment.

REFERENCES

1.1 Max Frank, "Exploratory Development of the Q-Factor Technique," Final Report on Contract AF 29(601)-6316, AFWL-TR-65-166, dated November 1965 (AD 476 408)

3.1 M. Yamin, "Charge Storage Effects in Silicon Dioxide Films," IEEE Trans. on Electron Devices, ED-12, pp. 88-96, March 1965.

3.2 P. J. Coppen and W. T. Matzen, "Distribution of Recombination Current in Emitter-Base Junctions of Silicon Transistors," IRE Trans. on Electron Devices, pp. 75-81, January 1962.

3.3 C. T. Sah, "Effects of Surface Recombination and Channel on P-N Junction and Transistor Characteristics," IRE Trans. on Electron Devices, ED-9, pp. 94-108, January 1962.

4.1 C. D. Taulbee, D. L. Nelson, B. G. Southward, "Effects of Ionizing Radiation on Transistor Gain," ASTM STP 384, "Radiation Effects in Electronics," pp. 121-148, May 1965.

4.2 A. F. Hogrefe, "Design and Packaging to Survive an Extended Mission in the Natural and Artifically Trapped Belts of Near Space."

4.3 D. L. Nelson and A. Hogrefe, Private Communication, July 1966.

4.4 D. L. Nelson, "Study to Investigate the Effects of Ionizing Radiation on Transistor Surfaces," Third Quarterly Report, May 1966, Contract NAS8-20135.

5.1 D. S. Peck, et al, "Surface Effects of Radiation on Transistors," Bell System Technical Journal, 42, p. 95, January 1963.

5.2 P. J. Estrup, "Surface Charge on Silicon Induced by Ambient Ionization," Solid State Electronics, 8, pp. 535-541, 1965.

5.3 A. Stanley, "Effects of Electron Irradiation on Metal-Oxide-Semiconductor Transistors," Proc. of the IEEE, 53, pp. 627-628, June 1965.

5.4 A. J. Speth and F. F. Fang, "Effects of Low Energy Electron Irradiation on Si-Insulated Gate FETs," Appl. Phys. Letters, 7, pp. 1945-1946, September 1965.

5.5 E. Kooi, "Influence of X-ray Irradiations on the Charge Distributions in Metal-Oxide-Silicon Structures," Philips Research Reports, 20, pp. 306-314, 1965.

5.6 A. S. Grove and E. H. Snow, "A Model for Radiation Damage in Metal-Oxide-Semiconductor Structures," Proc. of IEEE, 54, pp. 894-895, June 1966.

5.7 H. L. Hughes, "Surface Effects of Space Radiation on Silicon Devices," IEEE Trans. on Nuclear Science, NS-12, 53-63, December 1965.

5.8 A. Stanley, "Space Radiation Effects on High Gain Low Current Silicon Planar Transistors," MIT-LL Group Report 1965-11, Contract AF 19(628)-5167, February 1965.

5.9 D. J. Fitzgerald and A. S. Grove, "Mechanisms of Channel Current Formation in Silicon P-N Junctions," presented at Fourth Physics of Failure Symposium, Chicago, November 1965.

5.10 R. Williams, "Photoemission of Electrons from Silicon into Silicon Dioxide. Effects of Ion Migration in the Oxide," J. Appl. Phys., 37, pp. 1491-1494, March 1966.

5.11 R. Williams, "Photoemission of Electrons from Silicon into Silicon Dioxide," Phys. Rev., 40, A569-A575, October 1965.

6.1 P. J. Estrup, "Surface Effects of Gaseous Ions and Electrons on Semiconductor Devices," IEEE Trans. on Nuclear Science, NS-12, pp.431-436, February 1965.

6.2 R. R. Blair, "Surface Effects of Radiation on Transistors," AIEE 1963 Summer General Conference, Toronto, Canada.

6.3 H. L. Hughes, "Radiation Effects on MOS Devices," presented at Third Navy Microelectronics Conference, Monterey, California, April 1965.

6.4 A. L. Barry and D. F. Page, "Radiation Hardening of MOS Transistors for Low Ionizing Dose Levels," IEEE Trans. on Nuclear Science, NS-13, pp. 255-261, December 1966.

6.5 H. L. Hughes and R. A. Giroux, "Space Radiation Versus MOS Devices and Circuits," presented at Twelfth East Coast Conference on Aerospace and Navigational Electronics, Baltimore, October 1965.